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VOLUME 4 NUMBER 5
JULY/AUG 2008

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July/August 2008 Volume 4 Number 5

COLUMNS

DEPARTMENTS

ON THE COVER:
The digitized battlefield has become the Global Information Grid (GIG), where ground-, air-, sea-, and space-based assets interconnect via myriad networks. But while commercial technology gives us choices for *net-centric warfare*, COTS also provides ways to implement, manage, and test battlefield networks. See the articles starting on page 30.
(Images courtesy of DoD, U.S. Navy, and U.S.M.C.)

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Avionics bus interface evolution

By Duncan Young

Avionics buses are traditionally slow to evolve, partly because requirements change so slowly and partly because of the costs of development, certification, and sustainment. It is with the development of new airplanes that the demand for new bus architectures evolves. This can be seen in the adoption of Fibre Channel for JSF and ARINC 664, also known as *AFDX* for new Boeing and Airbus airplane types. Some buses, although ideally suited technically such as Time Triggered Protocol (TTP), have been sluggish to be adopted and might only find use in niche applications. However, although the rate of change might be slow, the nature of the market still leaves room for much innovation in packaging, soft cores, and test equipment by embedded computing vendors.

Avionics architectures typically separate the flight safety-critical elements such as primary flight control, cockpit, landing gear, and so on from less critical elements such as cabin environment, entertainment, and, in the case of military aircraft, the mission systems. This separation offers less onerous initial certification and allows incremental addition, as is often required for regulatory reasons, without the need for complete recertification. Significant savings in weight and power could be made with an integrated systems approach, using centralized computing supporting individual applications running in secure partitions with critical and non-critical data sharing the same bus. The most widely adopted of these is ARINC 664.

Other safety-critical bus technologies provide the same capability. For example, TTP is designed to provide time domain separation of groups of participants (such as nodes) on a bus. TTP can support a single fixed group or multiple groups; each participant within each group and each group are allowed time slots on the bus that are scheduled to ensure that every participant always has time to complete its data transfers. TTP can also detect whether scheduled participants are present and working correctly; it can detect transmission errors and tolerates faulty nodes. MIL-STD-1553B is similarly deterministic in its scheduling of bus traffic, but TTP is much more flexible and capable. However, MIL-STD-1553B is firmly entrenched in military avionics and mission systems. Because of this widespread use, it still remains the medium of choice for many upgrade and improvement programs.

Embedding MIL-STD-1553B

Typical COTS-based military avionics subsystems use modules such as VMEbus, CompactPCI, or VPX configured in an enclosure. It is a key requirement to add MIL-STD-1553B interfaces in a modular form to these subsystems, and the PMC form factor is the preferred choice. Other solutions include small mezzanines on SBCs or entire dedicated modules, adding eight or more dual-redundant interfaces into a single subsystem. But small-scale embedded subsystems can now be implemented as a System-on-Chip (SoC) using the latest generations of FPGAs. This creates opportunities for COTS vendors to offer 1553 IP cores for single or multiple remote terminals, bus controller, and bus monitor functions, extending the COTS value proposition well beyond the traditional board supplier.

Avionics interfaces on ExpressCard

With the continued development of new applications for avionics interfaces, bus analyzers play an important role in the testing and verification process. Similar to many market sectors, the laptop computer has become the ubiquitous test vehicle, easily supporting the four basic analyzer functions of display, logging and analysis, simulation, and playback when hooked up to a test rig or aircraft system. The laptop's PCMCIA slot has, until recently, been used to connect to the system under test. However, PCMCIA is rapidly being displaced by the new ExpressCard standard. This replaces the parallel interface of PCMCIA with PCI Express, offering significant improvements in performance and bandwidth plus compatibility with many other forms of embedded computing technology.

Despite its small size, an ExpressCard can support a dual-redundant AFDX port, logging all bus traffic, complete with 64-bit time tagging and IRIG-B for synchronization with external time sources. The RAF-EC AFDX ExpressCard module (Figure 1) is designed for use in avionics bus analyzers, along with its sibling ExpressCard products for MIL-STD-1553B and ARINC 429. The RAF-EC and MIL-STD-1553B soft cores are produced by GE Fanuc Intelligent Platforms.

Figure 1

While it appears that avionics buses are being left behind by the pace of technological change, there are sound economic and safety reasons why avionics architectures cannot change so rapidly. Appropriate new technologies such as TTP, developed for the automotive sector, are slow to migrate from their native markets even with proven certification to RTCA requirements. However, the pace of technological change will ensure that competitive innovation will continue to refine and improve the choices of avionics bus products available from the COTS market.

To learn more, e-mail Duncan Young at young.duncan1@btinternet.com.

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New FPGAs slot into heterogeneous DSP systems

By John Wemekamp

There is no doubt that FPGAs with their large arrays of multipliers have transformed the repetitive, parallel processing of sensor data at the front end of DSP systems such as radar, signals intelligence, and Electro-Optical/Infrared (EO/IR). Although earlier FPGAs offered the computational performance required, integrating the FPGA with the next level of processing while achieving optimal performance and dataflows required specialized skills as well as intimate application knowledge. The latest generation of FPGAs incorporates a much greater complement of high-speed serial I/O and embedded hard cores and/or vendor-supplied standard interface blocks such as PCI Express and Serial RapidIO. This makes them ideal for use within heterogeneous (mixed FPGA and processor) multicomputing systems. For maximum usability, this extra functionality must be supported by IP libraries and communications middleware to provide a flexible, high-performance dataflow architecture without the integration headaches.

Most military embedded computing applications have severe space, weight, and power constraints motivating designers to consider innovative remedies using the remarkable functionality of today's FPGA devices to achieve true System-on-Chip (SoC) solutions. However, complex sensor processing applications with many hundreds of channels and high data rates are unlikely to be resolved by FPGAs alone. While they are ideally suited to repetitive fixed-point algorithms such as convolution, filtering, and decimation, the resultant data streams will often need to be distributed to a further level of processing. In a large system, this would be an array of multicore Power Architecture processors with AltiVec vector processing enhancements. Such a mixed architecture is also better at supporting complex but variable processing solutions typically found in multimode radars, where an FPGA's reconfigurability can be exploited to optimize a radar's performance in different modes of operation.

Serial connectivity

In common with other embedded sectors, there has been a rapid migration of standards-based connectivity from parallel standards such as PCI and PCI-X to the serial connectivity of PCI Express, Serial RapidIO, and Ethernet. In the military embedded market, this has been facilitated by the introduction of the VPX (VITA 46) standard and the widespread use of Freescale Semiconductor's 8641D dual core Power Architecture processor, creating a new fabric-based framework for the implementation of complex multicompute node solutions. Through advances in process technology, the latest FPGA devices – such as Xilinx's Virtex-5 or Altera's Stratix IV – incorporate many more multipliers and logic elements. They also include a significant step forward in multi GHz, high-speed I/O signaling to satisfy the new serial fabric and networked vision of system connectivity. For example, the Virtex-5 includes up to four scalable PCI Express endpoints, configurable from x1 to x8 lanes, and Serial RapidIO soft cores, as well as up to eight 10/100/1000 Mbps Ethernet Media Access Controllers (MACs).

Military DSP solutions require advanced Direct Memory Access (DMA) controllers and banks of external memory (SRAM and DDR2 DRAM) to support the buffer sizes, dataflows, and fabric ports needed to process incoming streams of data produced by Synthetic Aperture Radar (SAR) or electronics intelligence gathering equipment. In the case of the multimode radar mentioned earlier, these dataflows may vary between modes in their bandwidth and routing, highlighting the need for the flexibility offered using a switched fabric compared to fixed, point-to-point links. But the key to making use of all this additional capability lies in a common interprocessor communications layer between all processing nodes within a system, whether FPGA or Power Architecture, and a set of IP cores and tools to ease their integration.

Together with the serial standards connectivity framework, these tools and IP make it possible to implement more efficient DSP solutions with mixed processing technologies, focusing on algorithm development, distribution of tasks, and dataflow rather than the time-consuming integration of disparate technologies. These principles are illustrated by the CHAMP-FX2 from Curtiss-Wright Controls Embedded Computing (CWCEC) shown in Figure 1. The VPX-compatible CHAMP-FX2 incorporates two Virtex-5 devices and a dual core 8641D processor, supported by Continuum FXtools. It includes IP in support of Serial RapidIO DMA engines, external memory controllers, and a scalable switching interconnect. All these are optimized for operation over rugged temperature ranges.

Figure 1

Today, many more mixed sensor/general-purpose processing applications are turning to FPGAs for an affordable, practical solution. Practical heterogeneous computing architectures will be the way to resolve the diminishing space, weight, and power versus performance dilemma. FPGA devices properly supported by COTS vendors' IP and tools, such as the Virtex-5 or Stratix IV, have the logical, arithmetic, and I/O capability to perform front-end DSP operations. In addition, they can slot into heterogeneous, serial-standards based computing systems, satisfying the military's complex future multicomputing applications.

To learn more, e-mail John at john.wemekamp@curtisswright.com.

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Legacy Software Migration

By Bill St. Clair

Legacy code in the security-critical age

The cost and convenience advantages of legacy code reuse can be diminished or complicated when security and safety-critical risks are considered. If the legacy code is proven to be functionally correct and operationally viable, its acceptance is based on an assumption of what is expected *to happen. However, it is the* unexpected *that typically causes faults, and structural testing provides a means of mitigating the unexpected.*

Today, the "as built" acceptance of legacy software is coming under more scrutiny. This is due, in both military and commercial systems, to an increasing emphasis on security and safety evaluation criteria. With respect to software aspects of certification, there is a mandatory requirement for evidence of a repeatable verification process and the analysis that supports it. *Structural testing* is a mechanism to validate this evidence.

Although once viewed as an unnecessary cost burden, a rigorous, standards-based development and verification process comes as a consequence of the emerging global perspective on the importance of safety in embedded systems industries worldwide. This perspective is defined by risks associated with activities as diverse as commercial air travel, medical equipment product deployments, global automotive product development standardization, and defense and security. In these applications, the liabilities, costs, and mission impacts associated with unexpected software and system behaviors are considered unacceptable.

As a member of the FAA's international working group on flight software, which is producing the next version of its DO-178 software standard, I have witnessed the growing awareness of the use of legacy software in flight software systems. The working group has strived to ensure that legacy code is properly managed, verified, and that it does not in fact become "dead" or inaccessible code where it could inadvertently be invoked for runtime execution without having been previously and properly tested. Historically, dead code has been seen as a cause of unexpected software behavior and poses a significant risk to flight safety.

With the emergence of object-oriented applications in embedded systems, using languages such as C++, Java, and Ada 2005, the working group has also realized that the possibilities for reuse of legacy code have grown exponentially. Legacy components can share member functions with new components, and the precise behaviors of these shared functions are not actually visible before runtime execution. In object-oriented systems, the unexpected has a higher probability of occurring.

The U.S. military also recognizes the risks associated with unexpected software behaviors, especially in the context of security vulnerabilities. The Air Force Research Laboratory, in cooperation with the National Security Agency, Department of Defense prime contractors, academia, and software suppliers, is managing a Multiple Independent Levels of Security/Safety (MILS) program to combine DO-178B with standards for security. This includes the Common Criteria and Director of Central Intelligence Directive 6/3, Protecting Sensitive Compartmented Information Within Information Systems. Though the MILS program does not directly address legacy code, many of its objectives are being applied to new projects and deployments that incorporate legacy software. The software development and verification guidance for the MILS program, which comes largely from DO-178B, now presents software suppliers and system integrators with the enormous challenge of implementing repeatable verification processes and mitigating the risks associated with unexpected software behaviors.

Given the challenges associated with security and safety-critical software, we need to identify best practices with respect to legacy code and propose a way to maintain and update legacy code. Such challenges are met through *structural testing.* Structural testing, sometimes described as "software testing software," provides a runtime environment in which test cases are auto-generated to exercise software behaviors based on a system-wide, path-level analysis of the code. Although in the past structural testing was criticized for not explicitly verifying functional correctness, this opinion fails to recognize that the goal of structural testing is to exercise the entirety of software structures, trap exceptions, and measure the resulting code coverage – *not* to explicitly test software functionality.

Unless the "as-built" architecture of legacy software is correctly analyzed, the impact of changes cannot be predicted nor can changes effectively be applied. Fortunately, the static analysis inherent to structural testing can also produce graphical representations of the architecture including call tree graphs, control flow graphs, data coupling tables, and set/used tables. These visualizations are especially helpful to engineers working with code from multiple origins such as modeling tools, hand code, and software libraries. Another byproduct of the static analysis dimension of structural testing is the automated application of coding rules to the source code, assuring implementation consistency between legacy and new code.

Advances in test technology have spawned a new generation of tools, not just another breed. These advances have arrived just in time to meet the needs of international software standardization, the globalization of embedded software markets, and the rising emphasis of security and safety-critical verification criteria. Now legacy software users can squeeze out unexpected software behaviors and help keep us safe and secure.

Bill St. Clair *is technical evangelist for LDRA Technology in San Bruno, California and has more than 25 years in embedded software development and management. He holds a U.S. patent for a portable storage system and is inventor of a patent-pending embedded requirements verification system.*


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Daily Briefing: News Snippets

By Sharon Schnakenburg, Associate Editor

www.mil-embedded.com/dailybriefing

Northrop Grumman and U.S. Navy want more

Northrop Grumman recently decided that enough *wasn't* enough, then granted a second (low-rate) initial production Central Electronics Chassis (CEC) contract to VMETRO, Inc. The contract stipulates that VMETRO provides three more CECs for the U.S. Navy's Airborne Laser Mine Detection System (ALMDS). CEC is a liquid-cooled ATR system, containing VMETRO's VPF1 quad processor payload cards and VITA 41 CSW1 switch cards. Meanwhile, the helicopter-deployed ALMDS program aids the U.S. Navy in spotting sea mines close to or at the surface of water by utilizing a blue-green laser and airborne light detection. Fifty-plus helicopter platforms are slated for ALMDS system outfitting.

Photo courtesy of Northrop Grumman

MicroTCA: Tough enough?

The debate of whether MicroTCA is really rugged enough – and for which apps – might be an open and closed case, according to Hybricon and Emerson Network Power. The closed case: Soon PICMG's MicroTCA.1 effort, which focuses on rugged industrial and commercial apps' shock, vibration, and extended temperature considerations, comes to completion. The open case: Work begins on the new PICMG Rugged MicroTCA.2 subcommittee, where Hybricon's Michael Palis serves as chair and Bob Sullivan takes on the secretary role, while Emerson's Stuart Jamieson is draft editor. Rugged MicroTCA.2 aims to address vibration and shock according to ANSI/VITA 47 for conduction- and air-cooled apps. The group will also focus on higher levels of harsh environment stressors than those covered by Rugged MicroTCA.1.

Static analysis is improving, report reveals

With backing from the U.S. Department of Homeland Security and as part of the government's Open Source Hardening Project, Coverity recently released its Scan Report on Open Source Software 2008. The report analyzes 55 million+ code lines from more than 250 open source projects utilizing the Coverity Prevent static analysis tool over a two-year timeframe. Projects analyzed include those implementing the Linux OS and Apache Web server, among others. Findings, related to the report's Scan site, indicated: There was a 16 percent drop in static analysis defect density; false positives detected by open source developers are less than 14 percent; and projects that have a large average function length are not more likely to have higher defect densities, among other findings. The free report can be downloaded at www.coverity.com.

Reducing SCA conformity risks

At the recent International Software Radio-Defence Conference held in London, Zeligsoft may have disproved the dangers of conformity. Case in point: Zeligsoft's new Code Generator v. 2.0 provides SCA device code generation, abstracting the physical radio hardware in compliance with SCA. This automated code production ensures that the platform continues to conform to the SCA specification during the full development cycle. Additionally, the company announced its SCA Core Framework (CF), an out-of-the-box solution comprising omniORB CORBA object request broker pre-integrated with the Zeligsoft CE system-centric development environment. Zeligsoft CE is geared toward software design for heterogeneous multiprocessor/multicore systems.

Lockheed Martin radar completes CDR

Getting critical isn't always a bad thing, particularly for military apps. A prime example is Lockheed Martin's (LM's) Enhanced AN/TPQ-36 counterfire target acquisition (EQ-36) radar, which has successfully completed its Critical Design Review (CDR). Consequently, the program's five radar systems are now set to start the initial production phase, with the first two systems slated for delivery to the U.S. Army by summer 2009, the third and fourth by fall 2009, and the fifth by early 2010. EQ-36 is touted to classify, detect, track, and determine locations of indirect enemy fire including artillery, rockets, and mortars in 360- or 90-degree modes. The EQ-36 will also replace outdated TPQ-36 and TPQ-37 medium-range radar, which offer only "limited" 90-degree operation. Total acquisition value could surpass $1.6 billion, LM reports.

SS/L sews up satellite modifications

Loral Space & Communications' subsidiary Space Systems/Loral (SS/L) recently delivered its tailored ProtoStar I satellite to Kourou, French Guiana. The satellite – spawned from an existing satellite purchased by ProtoStar – was altered to meet defined footprint/coverage and power requirements and deployed within 17 months of contract signing. ProtoStar I, operating on C-Band and Ku-Band, will offer two-way broadband Internet services to well-established and nascent Direct-To-Home (DTH) Asian market operators. The satellite is developed around SS/L's high-rel 1300 spacecraft bus and is anticipated to deliver 15+ service years. ProtoStar I, slated for launch onboard the Ariane 5 launch vehicle, is the first of several satellites on ProtoStar's docket.

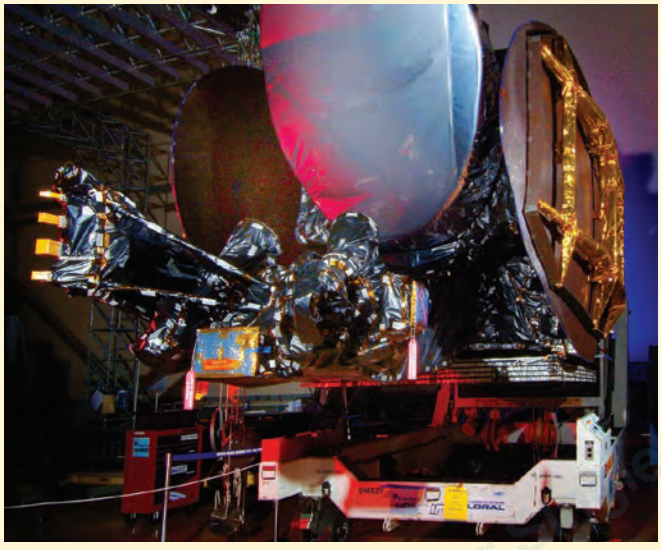

Photo courtesy of Loral Space & Communications, Inc.

It's not a world record ... or is it?

If the National Aeronautic Association (NAA) didn't see it, did it really happen? Boeing says so and has submitted their application to claim a world record to the NAA – the United States' sanctioning entity for the Fédération Aéronatique Internationale (FAI) – for a recent UAV flight. The A160T Hummingbird unmanned rotorcraft executed its 18.7-hour flight on May 14-15, thereby setting a world endurance record for its class (1,102 to 5,511 lbs or 500 to 2,500 kg), Boeing claims. "We didn't set out to establish a world record, but it was a great accomplishment," states Jim Martin, Boeing Advanced Systems A160T program manager. The flight occurred in southwestern Arizona at the U.S. Army's Yuma Proving Ground, where the aircraft transported an internal payload of 300 lbs at altitudes to 15,000 feet.

Photo courtesy of Boeing

Curtiss-Wright scores FCS contract win

Forming one piece of an integrated puzzle, an $8 million contract was recently awarded to Curtiss-Wright Corporation by General Dynamics C4 Systems and Rockwell Collins, Inc. The contract specifies that Curtiss-Wright provides its General Processor Modules (GPMs) for utilization within the U.S. Army's Future Combat Systems' (FCS') Integrated Computer System (ICS). The ICS synergizes 13 of 14 previously independent platforms within FCS, folding them into one secure, integrated computing environment. The initial order of GPMs is 1,000+ modules, expected to start shipping in Q2 2008.

Real-time image compositing:

Software displaces hardware for radar displays

By Dr. David G. Johnson

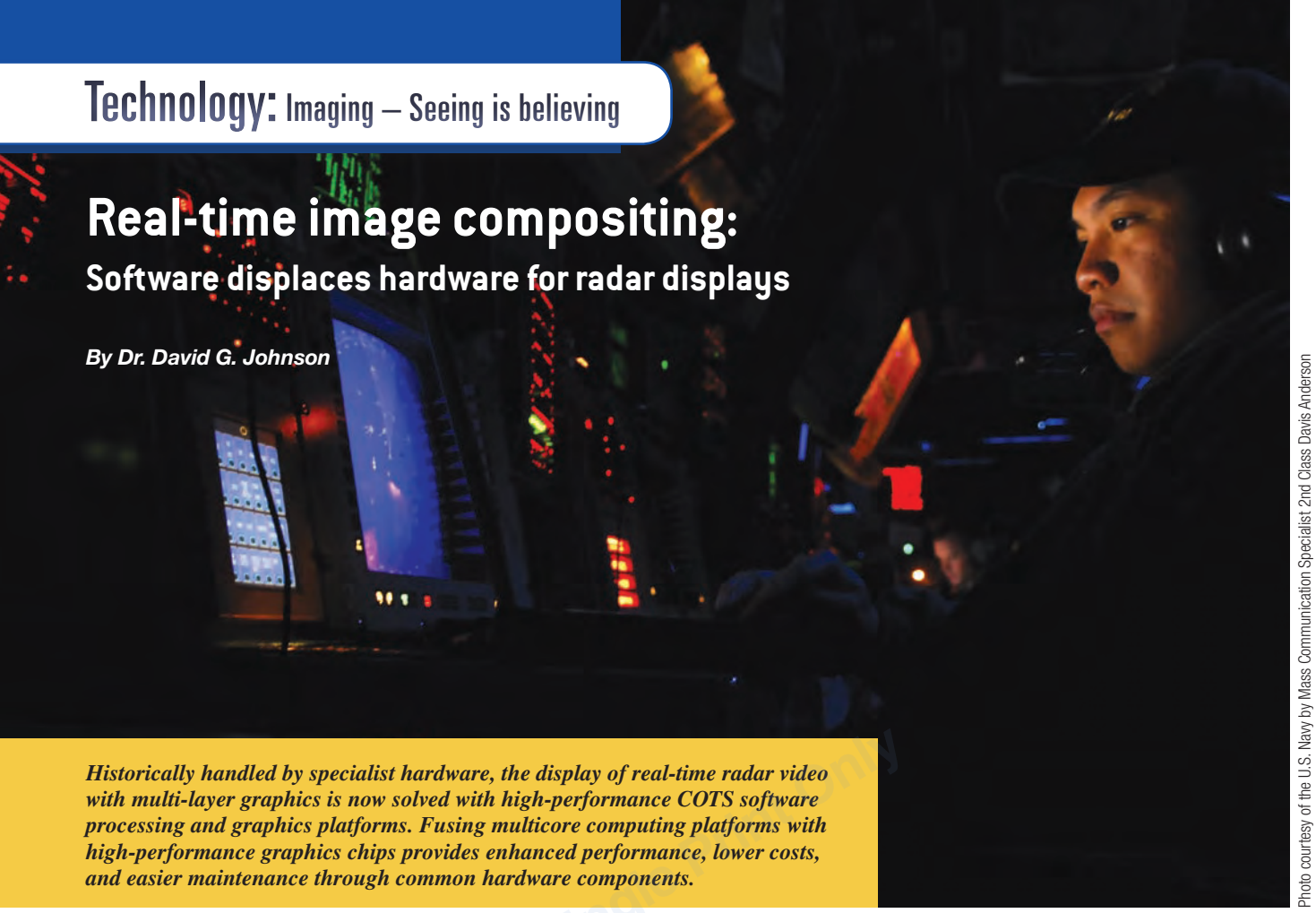

Photo courtesy of the U.S. Navy by Mass Communication Specialist 2nd Class Davis Anderson

Historically handled by specialist hardware, the display of real-time radar video with multi-layer graphics is now solved with high-performance COTS software processing and graphics platforms. Fusing multicore computing platforms with high-performance graphics chips provides enhanced performance, lower costs, and easier maintenance through common hardware components.

Military command and control displays combine radar video presentation with complex charts and overlay symbology for multi-layer display presentation. Managing the display's layers for timely updates and realistic radar presentation can present difficulties.

One approach to solving this challenge is to design special-purpose hardware display architectures that support multiple graphics layers. However, developments in COTS processing and Graphics Processor Units (GPUs) have enabled multi-layer displays to be implemented in software without compromising the quality of the display presentation. The new solution allows the compositing of multiple windows of radar video, along with underlay charts and overlay symbology, all updated at different rates and with minimal interaction between the display layers. An example of this is shown in Figure 1, which depicts a combination of underlay, radar, and overlay.

Standardized hardware platforms

A modern visualization solution for real-time data will employ all-digital processing and display. Sensor data may be supplied directly in digital format – commonplace for modern sensors – or may be converted from its analog legacy interface through a processing server. Standard Ethernet networks provide a cost-effective interconnect from sensors or processing servers through to multiple display clients, possibly incorporating video compression where the number of channels is large or network bandwidth is at a premium.

With the real-time video arriving at multiple display clients, it is highly desirable that the client architecture minimizes the need for special-purpose hardware such as a radar scan converter. These products have provided an excellent method for radar scan conversion and graphics mixing using innovative techniques, including multi-layer frame stores and video keying. However, if the solution to presenting combined graphics and sensor video could be achieved through software and standard processing and display hardware, the resulting client displays would be more cost-effective, smaller, and flexible. Furthermore, with the inevitable progression in processing and graphics

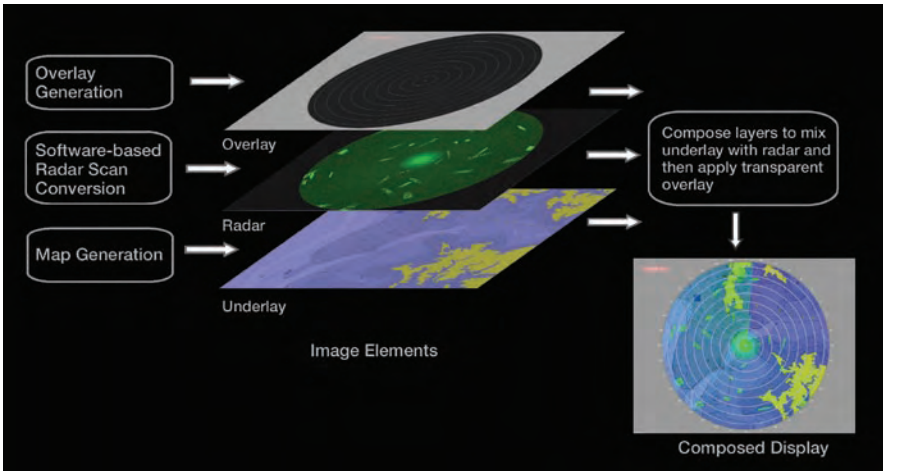

Figure 1

> “Furthermore, with the inevitable progression in processing and graphics architectures, software solutions support enhanced and evolving capabilities. In contrast, hardware solutions tend to solve today’s problem and offer limited growth or expansion potential.”

architectures, software solutions support enhanced and evolving capabilities. In contrast, hardware solutions tend to solve today’s problem and offer limited growth or expansion potential.

The need for specialized hardware in clients has tended to limit the capability of a console to reconfigure its role or evolve to new requirements. Often the hardware defines the function, and changes to the function will necessitate changes to the hardware. Furthermore, reduced hardware translates directly to lower maintenance costs and higher system reliability. Where the hardware has industry-standard computing and graphics hardware, the additional cost benefits and ease-of-upgrade serve to further reduce the lifetime cost of deployment.

Display presentation

The problem of displaying radar sensor video with graphics underlays and overlays is summarized in Figure 1, which shows a logical layering of graphical data with respect to the radar so that some graphics constitute underlay and others the overlay. The distinction of underlay, radar, and overlay in this manner is relevant only in defining the method of presenting the three elements.

The underlay element is likely a complex map composed of many logical layers that build up to form a naval chart. The method of combination requires the radar video to be mixed with the underlay element in a form of cross-mixing, in which pixel color depends on a combination of the graphics color and the radar color. In contrast, graphics drawn in the overlay element will be displayed in preference to any radar or underlay color at that point. It is only if the overlay presents a “transparent” color that the combined radar and underlay show through.

A convenient language and algebra for the description of image combination are provided by Porter and Duff in their seminal work on compositing digital images[1]. They describe the operations for combining images using logical operations, including blending, which they call the *over* operation. Applying this terminology to the display of radar video, we can define a combination rule that combines an overlay A with radar R and underlay B as:

$$\text{Display} = A \textit{ over } (R \textit{ over } B)$$

The *over* operator has an associated alpha component, which defines the degree

of transparency in the combination of two pixels. For the *R over B* operation, the combined radar and underlay graphic is computed from an alpha value that is computed for each display pixel to define the relative weighting between the two elements. This per-pixel alpha value has the requirement to leave the underlay graphics unaffected in the absence of radar, and otherwise display a proportional blend of the radar and graphics color.

The final *A over* operation demands an alpha value for A of 1 where the pixel is nontransparent and 0 where it is transparent. This implements a color-keyed overlay, where the combination ensures that the radar and underlay only appear when an overlay pixel is transparent. Figure 2 depicts an example where a set of three simple geometric shapes illustrates the combination effects. The combination of the three elements is a real-time process that needs to update the screen to provide smoothly updating graphics and radar video display.

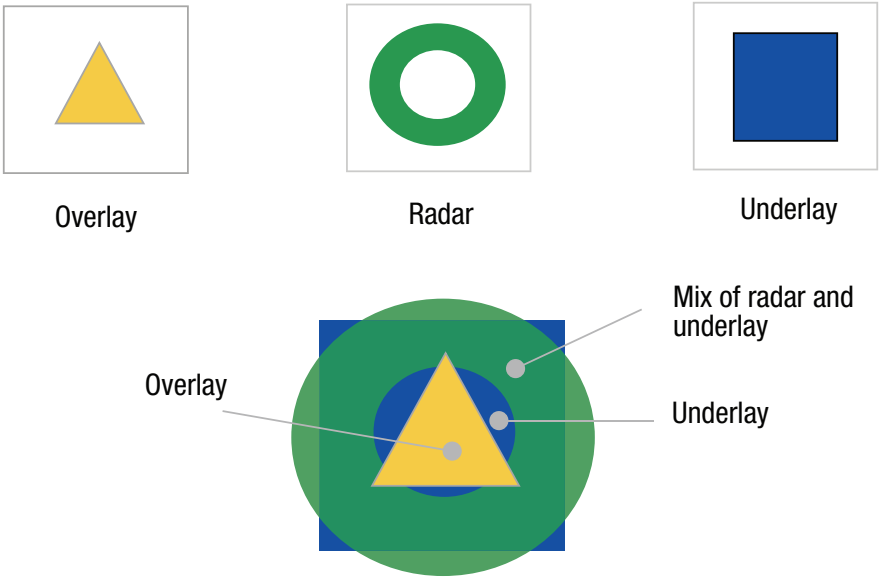

Figure 2

Finding a software solution

A number of developments in COTS hardware have enabled real-time software compositing to become a reality. First of all, the development of multiprocessor architectures with mainstream multicore processors provides enormous data processing capability. By designing the software to exploit the multiple processing elements, display-related processing can be allocated to one or more cores with minimal impact on other application processing.

The second development is in modern graphics card performance and architecture. Driven by the seemingly unlimited demands of gaming and simulation, the latest generation of graphics cards provides its own processing capability that serves to offload the main processor and accelerate graphics operations so they run entirely within the GPU's processing and memory subsystem. Significantly, the combination of a multicore processing platform and high-performance graphics subsystem is now an established computing platform available in ruggedized military form. One example is GE Fanuc Intelligent Platforms' MAGIC1 rugged display (see Figure 3).

Practical considerations

A practical implementation of a software-based, real-time image compositor has to do more than provide compositing functions for display elements. It has to work with the constraints of application software, third-party display toolkits, and graphics drivers. In the example shown previously, the underlay map comprises many display layers that may be constructed from a combination of raster and vector components. Such displays are commonly managed by third-party display toolkits, which handle complex display presentation. These toolkits are layered on top of the target computer's native window system, for example, Microsoft Windows or the X Window System for Linux and Solaris.

Application software that employs a toolkit for charting displays needs a radar scan converter and related display processor to present radar video in the layered method described previously. However, the interaction of the radar presentation and the graphical display toolkit needs to be minimal. The desired goal is that the display's graphical component can be managed independently of the radar layer, allowing the low-level graphical libraries to provide the necessary display combinations. Some situations may demand that the radar processing and display functions are handled in a different processing context (in UNIX terms, a *process*), providing protection against software failures.

Exploiting a software framework

Cambridge Pixel's SPx software framework provides a modern implementation of radar processing, distribution, and display that fully exploits the capabilities of modern processing and display hardware to offer multilayer compositing of real-time data (see case study, next page).

The software provides a capability to render complex, multi-layer graphics applications under both Microsoft Windows and X11 operating systems, supporting true multi-layer displays. The radar layer is updated at regular intervals to provide smooth sweep updates and realistic fading effects. The underlay graphics are mixed with the radar video, and the result is overlaid with another graphics layer containing symbology and track data. The software cleanly separates the radar scan conversion from the display processing, optionally allowing these functions to run on different machines.

An example of the performance achieved can be seen with a complex multi-layer underlay map (an S57 naval chart with 62 thematic layers, 1,400 point features,

Figure 3

4,000 line features, and 1,200 polygons), along with a real-time radar display (500 Hz prf, 4 second scan time). The radar display is updated at regular intervals of 20 ms to provide a highly realistic radar display sweep in 256 levels of radar color. Finally, the map and radar are overlaid with a range ring and target symbology that provides the overlay layer. This complete scenario runs on a rugged desktop computer with a high-resolution display of 1,600 x 1,200 x 32 bits per pixel and a Core 2 Duo platform (2.13 GHz processor) with an NVIDIA 7900 graphics card. The typical CPU/GPU load level is less than 10 percent, leaving ample resources for the application software.

SPx software provides flexibility in the display architecture, allowing the scan conversion of the radar video (the conversion from polar to screen) to be handled separately from the display processing, including the option to separate the function across a network. This allows centralized scan conversion of the radar video and distribution of incremental wedges of new data to the display consoles where the video is composited with the graphics layers. The software is easily reconfigured to move the scan conversion into the display console, distributing the polar video across the network if that configuration is preferred.

Industry standard provides best solution

By eliminating all special-purpose hardware from processing and display functions, industry-standard hardware and software components mean cost-effective initial deployment and an open-standards upgrade path for maintenance, repair, and upgrade. A network-based implementation shows radar video distribution from a central acquisition point through a display processor to a number of display consoles. The solution employs only industry-standard computing and display components to present the real-time, multi-layer display.

David Johnson *is technical director at Cambridge Pixel. He holds a BSc electronic engineering degree and a PhD in sensor technology from the University of Hull in the UK. He has worked extensively in image processing, radar display systems, and graphics applications at GEC, Primagraphics, and Curtiss-Wright Controls Embedded Computing. He can be reached at dave@cambridgepixel.com.*

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www.cambridgepixel.com

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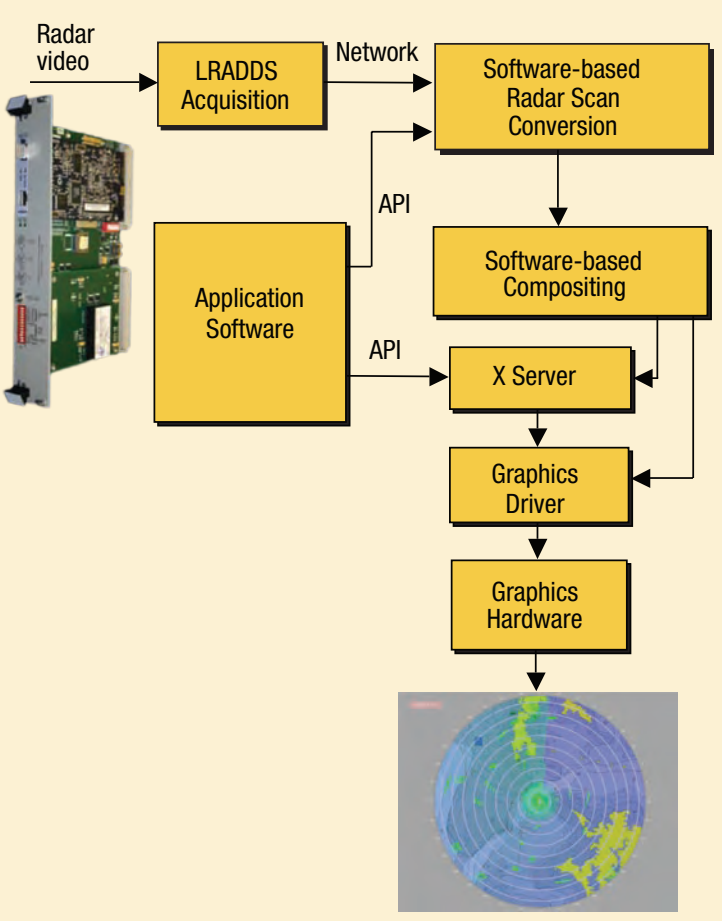
1. "Compositing Digital Images" T. Porter and T. Duff, *Computer Graphics,* Vol. 18, No. 3, 1984, 253-259.

Case study: Naval distribution for Frontier Electronic Systems

Radar video acquired from a number of sensors onboard a ship can be distributed using a product such as Frontier Electronic Systems (FES) LAN Radar Data Distribution System (LRADDS). Accepting a number of naval formats for radar input, LRADDS provides full bandwidth video on a standard Ethernet network for distribution and processing (see figure).

Cambridge Pixel's SPx radar processor, which uses only industry-standard computing platforms and display components, is capable of accepting LRADDS data and providing clutter processing and display enhancement capabilities before scan converting the data to a PPI display format. The scan conversion can either occur on the display client or, offering the benefits of distributing the processing load, can run on a dedicated radar video server. The server's output is the continually updating radar image, which is distributed to the display consoles for software compositing and display. The console provides a standard X Server for presentation of the underlay and overlay graphic components, with a client application managing the graphics independently of the radar video.



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Advanced image processing enables UAVs to fulfil their potential

By Doug Scott

Photo courtesy of NASA Dryden Flight Research Center by Lori Losey

Real-time image processing hardware has significant potential to efficiently and practically solve a number of problems currently faced by autonomous systems. A recent trial for autonomous airborne refuelling has demonstrated the potential – and great success – of applying image processing to an extremely challenging problem.

There are many reasons why Unmanned Aerial Vehicles (UAVs) are attracting so much interest – and investment – from military organizations around the world. By not endangering a pilot's life, they can fly missions that would otherwise be judged too dangerous. True autonomy – the goal of much UAV research – allows an overall reduction in personnel. And the fact that mission length is potentially not a function of pilot fatigue is highly attractive.

However, mission length – until such time as solar power becomes a viable alternative – is compromised not only by pilot-related factors, but also by the need to refuel. The ideal UAV will never need to return to base for refuelling, and this requirement has been at the heart of substantial research into in-flight refuelling.

Much development effort has been expended on the potential for GPS technology to enable a refuelling tanker and a receiver UAV to move within close enough proximity of each other to allow docking the fuel probe into the UAV drogue. However, the degree of precision required – especially as either craft is vulnerable to disturbance factors such as turbulence – is at the very outer limits of GPS accuracy. An alternative technology – the use of advanced image tracking and image processing systems – needed to be developed to complement the GPS system to enable a complex, highly sophisticated maneuver (Figure 1).

Evaluating that alternative was the goal of a joint project Advanced Airborne Refueling Demonstration (AARD) developed by the Defense Advanced Research Projects Agency (DARPA) and Sierra Nevada Corporation (SNC). The combined effort produced the first successful demonstration of autonomous probe-and-drogue airborne refuelling, and was conducted at NASA Dryden Flight Research Center.

DARPA and SNC settled on using the probe-and-drogue (or hose-and-drogue) refuelling method in the demonstration because it is widely perceived as the most difficult to automate – a function of the flexibility of the hose and its susceptibility to aerodynamic disturbance. Octec – now part of GE Fanuc Intelligent Platforms – and Sierra Nevada Corporation teamed to develop and deliver the image capture and processing functionality that was central to the demonstration's success.

The challenge

At the project's outset, a number of key studies had to be executed which, in cases such as determining the optimum viewpoint location for the image tracking device and ascertaining the ideal field of view, were interrelated.

Among these studies was an evaluation of alternative image capture approaches. It was known that whichever technology was chosen, the requirement would be to provide a range measurement accuracy of approximately 36 inches at a range of 100 feet to establish the relative positioning of the probe and drogue, closing to an accuracy of 4 inches at a range of 12 feet to allow probe insertion.

Key considerations in selecting the image capture device and the medium used to transmit the captured image data for processing included:

- The resolution of the captured image
- The ruggedness of the device
- Size and weight
- Susceptibility of the transmission medium to the ElectroMagnetic Interference (EMI) that could be expected to be present in an RF-rich environment

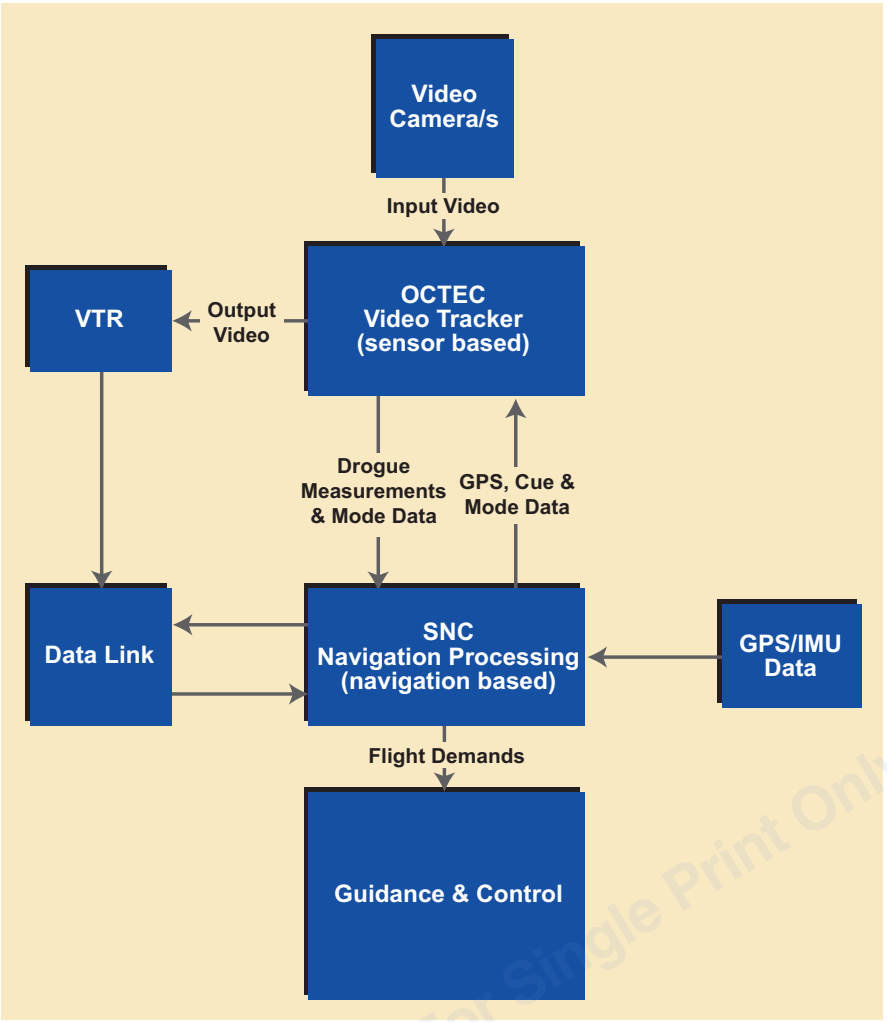

Figure 1

It was determined that a high-resolution digital sensor would be the ideal solution; however, its adoption was precluded by any amount of development time necessary to customize the tracker hardware to meet the sensor's digital interface standard. While a high-density fiber optic transmission line was believed to offer the optimum resistance to EMI interference, testing revealed that it gave such a poor image resolution that it was not possible for the tracker to detect a several-pixel object at the extended 30-meter range. The fiber cable also suffered from a relatively large number of dead pixels/fibers.

Finally, a standard NTSC video camera was found to deliver sufficient image resolution to resolve the drogue and basket at a range of 30 meters. A "remote-head" version of the camera was selected to minimize the size and weight impact at the chosen mounting point. The associated transmission cable was shown to offer acceptable resistance to EMI, and the video quality did not indicate any noticeable image interference artifacts.

Evaluating alternative sensor-mounting positions

Although the application is ultimately intended for completely unmanned platforms – both the refuelling tanker and the UAV – the demonstration took place using a manned NASA F-18 flight research aircraft (pictured, first page of article). The four optimum locations for the remote sensor on the F-18 were identified by the NASA flight crew, but modelling and simulation of the desired flight profile and viewpoint constrained the selection to two. The Head Up Display (HUD) view gave close operating range to the drogue and offered the maximum likelihood of the drogue being within the field of view. The view from the inboard right pylon gave good drogue visibility in the terminal phase and had the advantage of being an existing camera position. Both mounting points, however, also had disadvantages that needed to be factored in.

These disadvantages were driven to a large extent by the fact that the tracking algorithm required a minimum of several

pixels on the drogue target for recognition and tracking; this, in conjunction with the NTSC sensor's resolution capability, dictated a maximum Field Of View (FOV) of 55°. Too narrow a point of view would make acquiring the drogue more difficult and would also cause problems as the drogue came closer, filling the entire field of view. Within the event, the optimal field of view was determined to be 55°.

For the demonstration's purposes, two camera positions were used primarily to evaluate their effectiveness. However, deployment of the image-processing hardware within a UAV environment requires only a single camera, minimizing weight and power consumption and avoiding further complexity arising from installing two or more camera sensors at multiple locations on the airframe. This was possible because of the significant development effort in creating algorithms that can accurately estimate range from a single camera.

Provisions were also made in developing algorithms to eliminate background clutter that could be mistakenly identified in the captured image. For example, some of the aircraft structures such as the engine exhaust nozzles and fuel hose exit aperture, under certain lighting conditions, appear very much like the drogue at extended distances. Areas behind the tanker that should be avoided – described as "avoidance volumes" – were determined through simulation.

Another challenge in accurately identifying the position and distance of the drogue relative to the hose resulted from trial video analysis. This showed that the instability of the drogue's outer rim (Figure 2) made it an inappropriate reference point. However, the drogue's solid inner hub was found to exhibit stable high contrast, making it relatively easy for the sensor to identify and providing a practical calibrated reference point.

Figure 2

Measuring range from a single camera

A significant effort was expended to develop the appropriate range estimation algorithms, and two were proposed. One was based on a classical centroid approach; the other was a model-based approach. The algorithms were implemented in MATLAB and tested against the simulated models.

It was determined that each algorithm has complementary strengths and weaknesses. The centroid-based approach delivered superior resolution due to its measuring an area in image pixels, while the model-based approach was more stable and more accurate by comparing the observed video pattern with a known reference.

Figures 3a and 3b show the reported estimates from each algorithm against a known true range for each image field in the video sequence. As expected, the model-based approach is noisier at the further ranges than the centroid-based approach; however, the centroid-based algorithm suffers from gain and offset bias in its ability to measure accurately.

The decision was made to implement both algorithms running in parallel. This resulted in a measurement accuracy better than 10 centimeters from a range of approximately 3 meters. Desired accuracy was originally specified as 1-sigma (that is, 68 percent of the time) standard deviation; the accuracy achieved was predominantly better (that is, it was within the given range about 90 percent of the time – almost 2-sigma standard deviation).

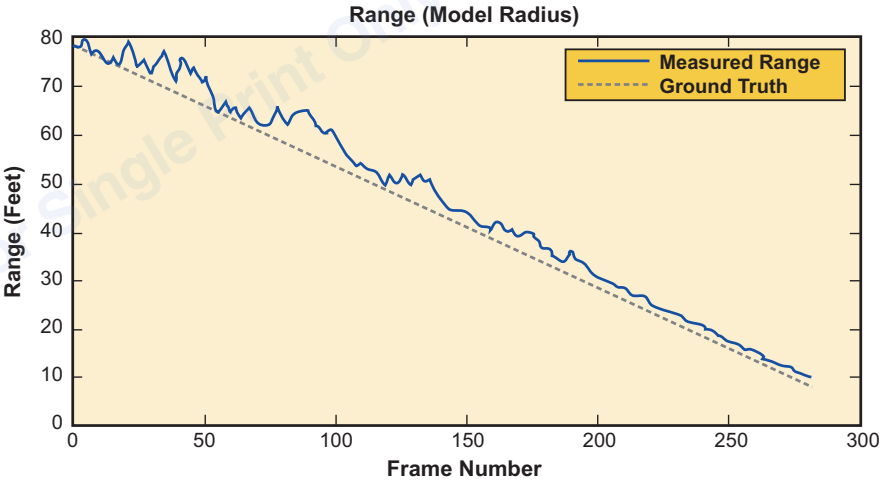

Figure 3a

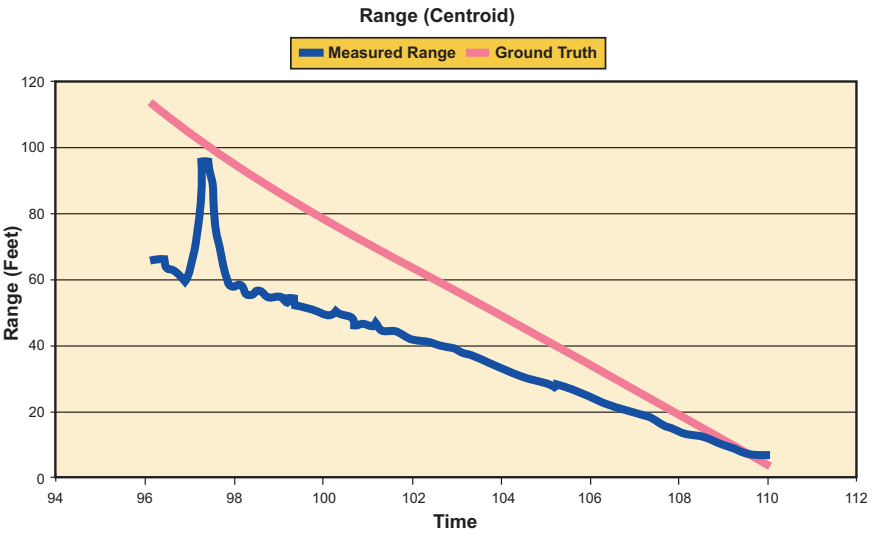

Figure 3b

> "As expected, the model-based approach is noisier at the further ranges than the centroid-based approach; however, the centroid-based algorithm suffers from gain and offset bias in its ability to measure accurately."

At the heart of the automated airborne refuelling demonstration was Octec's ADEPT-60 sensor-based video tracking and image processing module (Figure 4). It is natively equipped with several image processing algorithms and extended to enable the measurements from the newly developed algorithms to be combined. This provided the flexibility to optionally estimate the range without direct interaction between the underlying algorithms.

The increasing proportion of the field of view occupied by the drogue as it moved closer to the refuelling tanker – from a few pixels at a distance of 30 meters to more than half the field of view during the docking phase – led to the requirement to modify the tracking algorithm to contain a resizable image template of the target in memory, which is dynamically updated using the estimated drogue size. The template image also served as a first-stage mechanism for reacquiring the drogue in the event of an intermittent track loss.

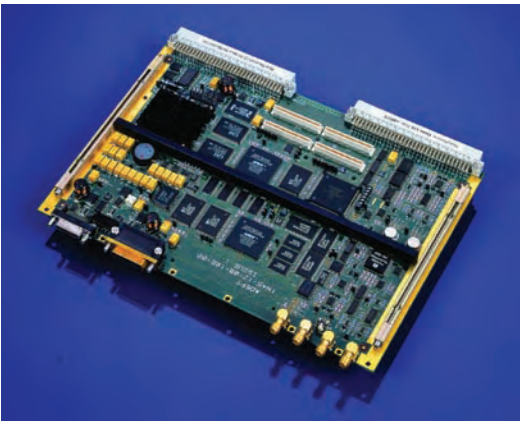

Figure 4

As noted earlier, the selected mounting points for the image sensors were not without their drawbacks. Most significant among these was a concern that the HUD cockpit window would induce significant image distortion. This issue was addressed by calibrating the system using "real world" measurements of various 3D points around the aircraft and hangar, and tracking these same points through the image capture sensor. An optimization routine was written in MATLAB to model the camera and lens parameters, and the known 3D points were reprojected through the model and compared with those measured by the vision system. This allowed the processing algorithms to be modified to compensate for anomalies in the camera's field of view.

The next phase

The demonstration proved that the application of advanced vision-based sensors for image capture and state-of-the-art image processing technology to augment the existing capabilities of sophisticated GPS-based positioning systems can be achieved. However, work to maximize the viability and deployability of this technology continues. Overall performance in acquiring the target image can be increased. Operating range – the initial distance at which the drogue can be captured – can also be extended, reducing the reliance on very precise GPS-based measurements. Finally, work will be done to enable drogue type identification, recognition of anomalous drogue behavior, and the effects of lighting and weather conditions.

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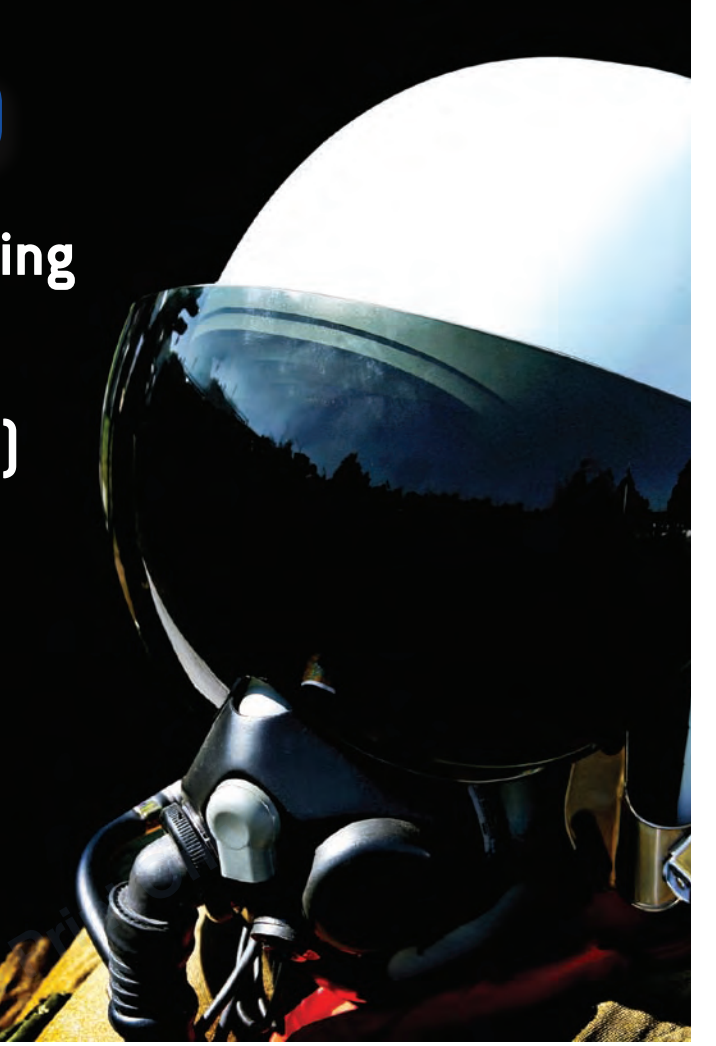
Remote Monitoring Debriefing System (RMDS) conceived and developed by the Israel Aircraft Industry (IAI)



By Yehuda Singer, PhD

The Remote Monitoring Debriefing System (RMDS) is intended for the first solo flights of a pilot trainee. It enables the trainer to monitor the flight in real time and to play back the flight later to provide detailed feedback and instructions. The system performs: 1) flight planning; 2) real-time flight monitoring; and 3) post-flight processing and comparison of the intended flight plan to the performed flight simulation.

Yehuda focuses on real-time flight monitoring and shows the system analysis process that led IAI & Beyond2000 to choose a dual core DSP architecture based on Analog Devices' BF561.

A pilot trainee performing his or her first solo flights could commit errors that could lead to serious accidents. A simple solution is to put a video camera in the cockpit and transmit real-time video to the trainer monitoring the flight from the ground. However, the transmission of a digital video at the rate of 15 frames per second necessitates bandwidth of 160 Mbps. The cost of such a channel is prohibitively expensive. The question is how to avoid transmitting video and still monitor the state of the aircraft in flight. The solution is to perform image processing on the input video and transmit numerical results to the ground. Transmitting numerical results requires a bandwidth of only 9,600 bits per second, which is easily and economically transmitted over an RF radio modem (see Figure 1).

Figure 1

Figure 2 shows the system operation during flight. The aircraft is equipped with cameras connected to the cockpit video processor, a radio modem, and a GPS. The cockpit video processor performs image processing to analyze the state of the meters. The numerical results of the image processing and the GPS data are sent via the radio modem to the Ground Station (GS),

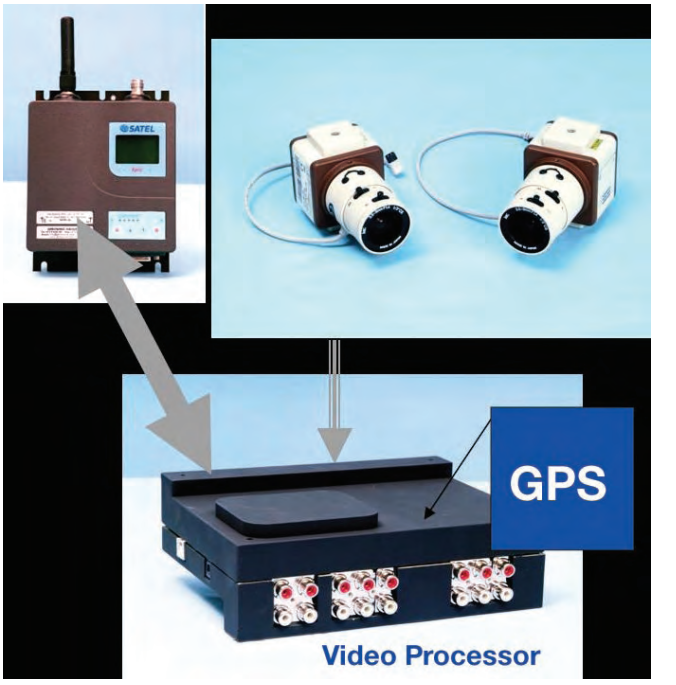


Figure 2

which restores the view of the panel and the 3D map as closely as possible to the real view seen in the aircraft. The platform of the GS is based on the FSX-Microsoft Flight Simulator.

To achieve a ground that is as close as possible to real video, we need to perform image processing at the rate of 15 frames per second on each camera.

System analysis

At the system analysis stage of the project, the computer requirements are:

1. CPU load is 30 percent
2. The bandwidth of the memory and bus is 40 percent

The assumptions for estimating the usage of these resources are:

1. The image processing is performed on a set of Regions Of Interest (ROIs)
2. Each ROI is 100 x 100 pixels = 10^4 pixels
3. There are 20 ROIs
4. 15 frames per second
5. Memory access of 10 ns, which relates to failure in accessing the cache memory.
6. A CPU faster than the memory is delayed by the memory whenever it accesses it.

Therefore, to estimate the CPU load, we have to count the number of memory accesses in our algorithm. Since the algorithm does not access the memory sequentially, we take a larger value of the memory access time. Table 1 shows the CPU load, which is much higher than desired: more than 54 percent compared with the value of 30 percent corresponding to the typical requirements. Table 2 shows the required memory bandwidth. It is a little more than 40 percent.

Function	Memory accesses	CPU load in 1 second
Threshold	2 x 15 x 20 x 10^4	0.06
Contrast	2 x 15 x 20 x 10^4	0.06
Vibration	10 x 15 x 20 x 10^4	0.3
Identification	4 x 15 x 20 x 10^4	0.12
Total	18 x 15 x 20 x 10^4	0.54

Table 1

Function	MBps
Video in (2 x 15 frames, 525 x 858)	25.76
Video out	12.88
Internal memory transfer	2.86
Total	41.5

Table 2

In the next section we shall introduce other considerations in choosing the computation platform for our project.

Choosing a platform

Software development associated within such a project is the critical path; hence, the requirement was to find an off-the-shelf evaluation board with two processors and start the software development without any wait for hardware development. At the end of 2004, we chose the Analog Devices BF561 dual-core as a platform for our project. By choosing the BF561 (see Figure 3), we removed the bottleneck of CPU time.

Memory bandwidth is supported by:

1. A separate cache for instruction
2. A separate cache for data
3. A fast DMA to capture streaming video in and out.[1] (In addition, the BF561 has standard I/O resources such as RS-232, SPI, and parallel I/O)

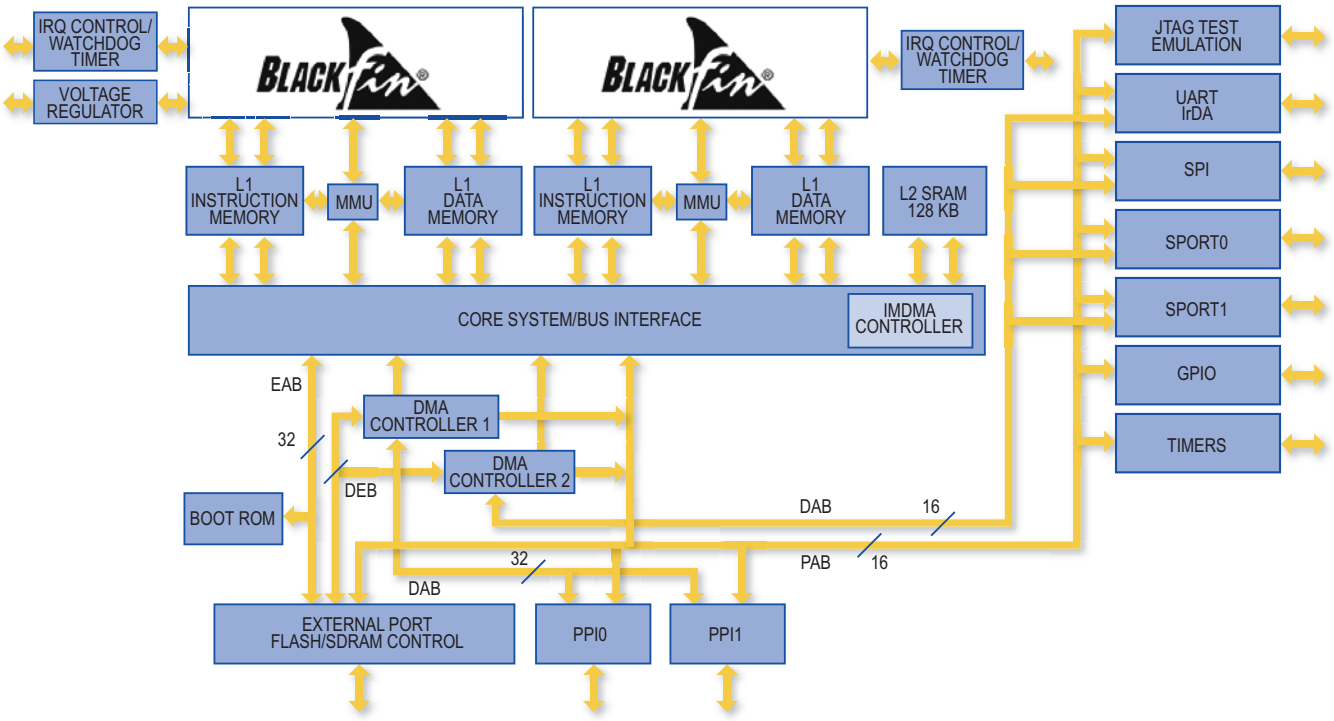


Figure 3

[1]Video out is needed for debugging purposes.

Analog Devices' evaluation board, the ADSP-BF561 EZ-KIT Lite,[2] enabled us to start software development immediately. I/O not included on the evaluation board was implemented on an extension board connected to the evaluation board via backward connectors.

The software tools associated with the BF561 permit one PC to serve as a development platform controlling the two DSPs (see Figure 4). Of course the software development process of a multiprocessor becomes simpler when the development system is controlled by one PC. In addition, software development of a real-time image processing application implies supporting utilities to the Integrated Development Environment (IDE). It is necessary to display the input image as sampled by the video decoder in the DSP. Figure 5 shows an image captured by the video decoder and stored in the DSP's memory. The image is displayed by the image viewer, which is a part of the IDE. This feature helped in integrating progressive scan video cameras. The progressive video is essential in image processing applications in a vibrating environment. The camera produces a TV standard that is 525 lines and 858 columns. The image produced by the camera is at the size of 640 x 492 pixels per frame. The image viewer helped in finding the input video's real size, which is 525 x 858.

Software design to enhance performance

The two cores interact via a shared memory. The shared memory is an external DRAM controlled by external port flash/SDRAM (see again Figure 3). The utilization of the two cores depends on the functional decomposition of the project. In an ideal situation when the computation task can be decomposed into independent subtasks, the processors are fully utilized. On the other hand, if the functional decomposition yields interdependent subtasks, much time is spent on synchronizing the processors in accessing the data in the shared memory. The design goal

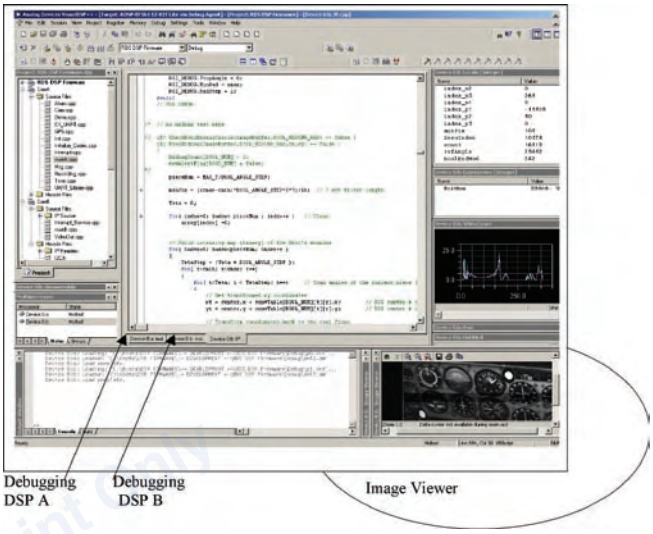


Figure 4

[2]We used the evaluation board as a part of the first prototypes delivered to the first customers and for the experimental flights.

is to minimize these interdependencies; hence, the processors become loosely coupled.

Figure 5 shows the functional decomposition of our system. Each DSP has its own cache memory instruction and cache memory data. One DSP samples the video from the camera and performs image processing only, while the second DSP interfaces the external world:

1. To the GS via the RF modem
2. To the GPS
3. To the contrast control of the cameras

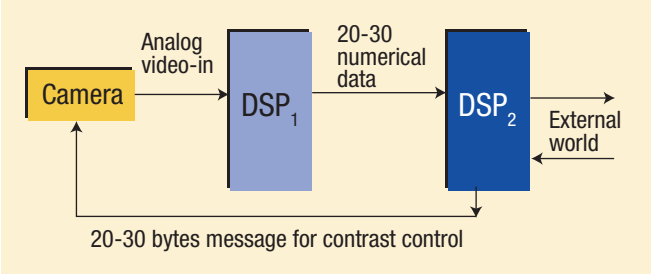


Figure 5

The DSP performing the image processing handles the second DSP with numerical results and the contrast values via the shared memory. The second DSP does not acknowledge the acceptance of these data, reducing our synchronization costs.

This functional allocation of tasks to the two DSPs guarantees that they are loosely coupled; thus, their computational power is maximized.

Video processing

The streaming analog video is captured by the video decoder, which converts it to digital and transfers the converted video to the external memory by one of the DMA channels. When a frame is completed:

- An interrupt is generated to the DSP when a new frame has been received and is stored in memory.
- DMA switches automatically to get an additional frame in a new memory buffer without the interference of the DSP.

The DSP processes the frames concurrently while new frames are captured by the video decoder. To enhance performance, portions of the images that relate to the ROIs are transferred from the DSP's external memory to its internal memory.

To enable debugging in real time, we produce an image with video markers on a monitor TV that shows the last frame processed. However, our input video is a progressive scan type, while a monitor TV supports interlaced video.

Figure 6 lists line information on the two types of video. A progressive scan video frame is composed of a contiguous sequence of 525 lines starting at line 0 and ending at line 524. An interlaced video is composed of two subframes: One subframe is a sequence of all even lines starting at line 0 and ending at line 524; the other subframe is a sequence of all odd lines starting at line 1 and ending at line 523. We again used the fast DMA that is part of the BF561 to convert the progressive video to an interlaced video. In addition, we added special markers to show the results in video for debugging and recording for debug purposes.

Progressive Video	Interlaced Video
$Line_0$	$Line_0$
$Line_1$	$Line_2$
$Line_2$	$Line_4$
$Line_{262}$	$Line_{524}$
$Line_{263}$	$Line_1$
$Line_{264}$	$Line_3$
$Line_{524}$	$Line_{523}$

Figure 6

Audio handling

To enable communication between trainee and trainer outside the normal avionics communication channel, we added voice handling via the radio modem. The radio modem works at the baud rate of 9,600 bits per second. The bandwidth for the voice is 3,200 bits per second from the global baud rate of 9,600. The solution is to perform compression and decompression in the DSP that interfaces with the external world. The trainer has a microphone and an earphone connected to the GS. The GS compresses the trainer's voice and sends it via the RF modem to the BF561; the BF561 decompresses and activates the audio decoder, which is connected to the trainee's earphones. The trainee can speak to the trainer through his or her microphone, and the BF561 compresses his or her voice and sends it via the RF modem to the GS. In the GS, voice restoration is performed and routed to the trainer's earphones. The convention in avionics systems is half-duplex communication. Voice handling involves interacting with the audio code, Serial Port (SPORT), and the DMA. The digital interface of the audio codec is the SPORT. Audio streaming is supported by the DMA.

Project status

Our version of the project is now working. The BF561-based system performs image processing at the rate of 14.7 frames per second; the numerical results are transferred via the RF modem to the GS, which restores the panel and the 3D and 2D maps. The computing load of the BF561 is around 80 percent. Now we are working to optimize the code and enhance internal memory usage by transferring only the regions of interest of the frame to the internal memory. Our goal is to reduce CPU load to 40-50 percent.

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Implementing net-centric tactical warfare systems

By Gordon Hunt

UAVs lend battlefield insight

A primary function of UAVs is the collection and communication of real-time battlefield information into the net-centric view. General Atomics Aeronautical Systems Inc. is a renowned market leader with its Predator, Predator B, Sky Warrior Alpha, and Sky Warrior Block 0 UAVs. They have adopted a data-oriented development model to enable a single Advanced Cockpit Control System to interface to these UAVs' telemetry systems. The cockpit includes a Common Operating Picture to assist the pilot in understanding the combat situation, facilitating a higher-level view of the battlefield than just a streamed video feed (see photo above).

Net-centric battlefield systems abstract data away from individual devices and provide a common infrastructure for disparate systems to exchange data across the tactical environment. Net-centric principles – making use of data-driven approaches such as those used in the Object Management Group's (OMG's) Data Distribution Service (DDS) standard – are being implemented in a variety of both new and existing tactical weapons systems. Better data exchange standards are also essential in driving the vision of the net-centric battlefield.

The tactical battlefield has long been characterized by the use of many different data collection and analysis systems that present information on small and discrete areas of the conflict to separate command and control stations. The operators of these stations attempt to use that data to estimate enemy intentions and actions, and counter with manual direction of the equipment and personnel in a simulacrum of coordinated response.

However, these individual systems are typically focused on their individual missions, rather than on strategic coordination to achieve a larger objective. When these disparate systems are integrated, it is often with a particular mix and mission in mind. Each system, whether tank or aircraft, for example, is extremely capable and can win their individual battles, so to speak, yet lose the war due to a lack of coordinated activity.

One way to dramatically improve the speed-of-command on the battlefield is to create a data-centered net-centric battlefield operation (Figure 1). Each individual element of a tactical system performs its narrow mission, but shares data as needed with others in a way that provides a more complete and accurate representation of the battlefield environment and the role of that system in the environment.

In the past, systems have been designed with point-to-point data communications that focus on delivering data from the sensor directly to an operator. In these cases, the endpoints are known to both producer and consumer, and the data format is agreed upon and unique.

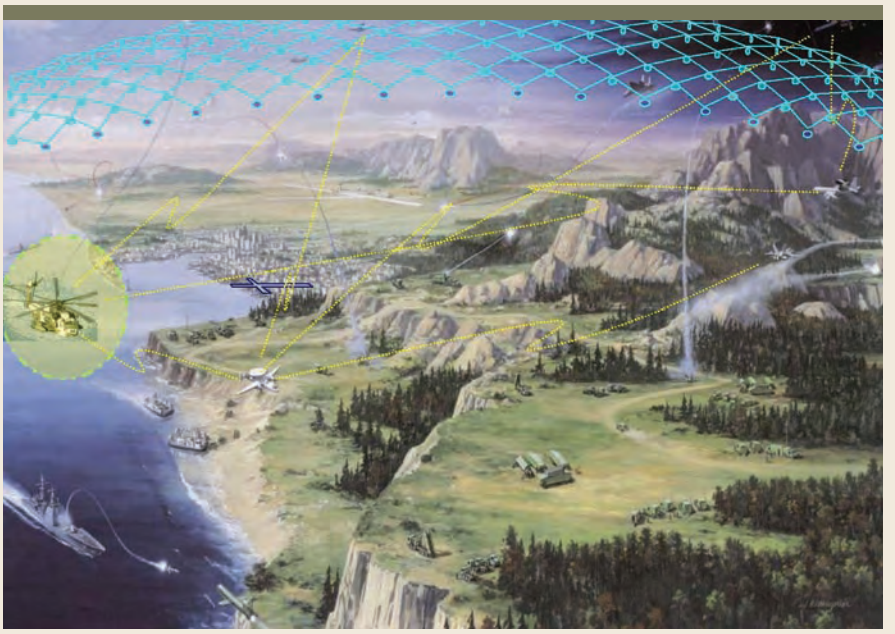

Figure 1

Point-to-point connections between individual systems are fragile and certainly don't meet the requirement for dynamic data integration between multiple systems. The correct approach is to provide real-time connectivity to all systems within the battlefield framework, and to move the limited intelligence and data away from the individual system and onto the network as a whole. Once the data, such as position, radar signals, and ground intelligence, is abstracted from the individual system and made available across the network, numerous applications can be written to analyze and act on it, providing a significantly higher-level view and a faster response time.

The validity of this data-oriented architecture for net-centric system deployment has been proven by the OMG Data Distribution Service, built around an open-standards data-centric model. Commercial Off-The-Shelf products that have implemented the OMG DDS standard have been used in a growing number of both new and existing weapons systems projects with great success. These systems are particularly adept at coordinating, analyzing, and responding to data across large-scale networks where response time is critical and resilience to battlefield events is mandatory. If, for example, radar data indicated an incoming missile, targeting and fire control can receive that data and use it for countermeasures, even though the radar and fire control systems were not originally designed to work together. The only limitation to scalability of the DDS middleware is in the physical limitation of the network architecture.

A key enabler of the resilience in these systems is the rich set of DDS definitions of application-level Quality of Service (QoS). Every producer and consumer of data to the global data space defines their service capabilities or requirements through a QoS contract broker, and DDS ensures there is a match before the communication is established. Even if the data is available and the contract of service between producer and consumer is broken, by using one of the QoS features an alternative data supplier will be automatically sought by the DDS middleware.

Achieving net-centric goals in a battlefield environment

Net-centricity through the use of data-enabled battlefield systems and a comprehensive data-distribution system is not merely a theory or abstraction. Weapons systems have been putting it into practice with new development efforts as well as existing system modification projects.

An example of such a system enhancement is the Navy E2-C Hawkeye. The Hawkeye provides all-weather airborne early warning and command and control functions for the carrier battle group. Network and system upgrades for this venerable weapons system include the addition of middleware incorporating the

tenets of data-centric design, performance optimization, portability across existing and future architectures, hardware and operating systems, as well as security best practices as defined by Common Criteria Information Assurance.

The goal of the development effort was to provide a platform by which data from the many radar systems and sensors onboard the Hawkeye platform can be aggregated for analysis of signals to determine the extent of a threat, and to suggest action for neutralizing that threat. (Figure 2 depicts the Hawkeye Software design after DDS had been used to implement a data-oriented communications model.) By abstracting the data and the data's QoS away from the application layer and into its global data space, current systems as well as future enhancements can leverage the data, not worrying about data source implementation details.

In a similar manner, the Navy Open Architecture program is a foundation for the modernization of the Navy's cruisers and destroyers, including the Aegis upgrade, the Total Ship Computing Environment (TSCE), and the Littoral Combat Ship (LCS). The Open Architecture program incorporates Data Distribution Services that enable the on-time delivery of data across the network to the subscribing components, even if they change during the course of system upgrades and enhancements.

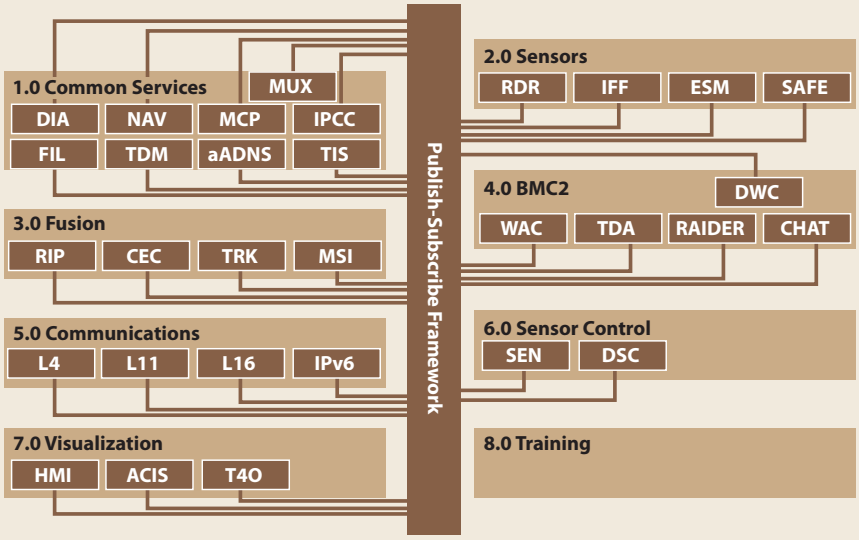

Figure 2

The Open Architecture program has been commonly implemented through network middleware that uses a publish-subscribe

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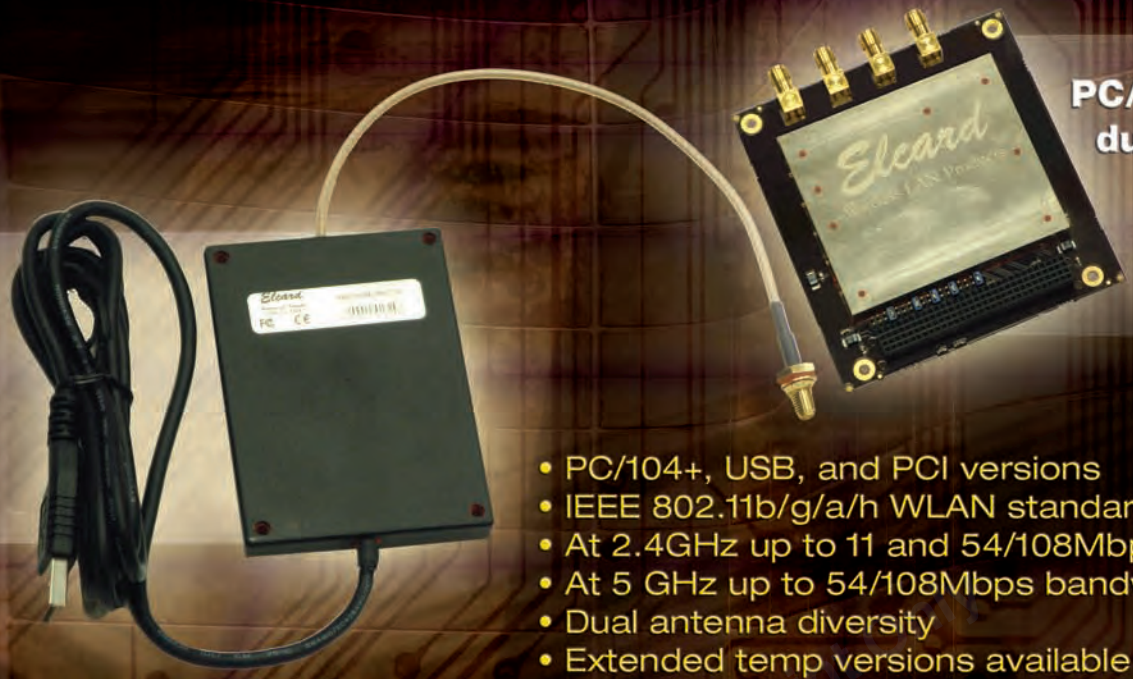

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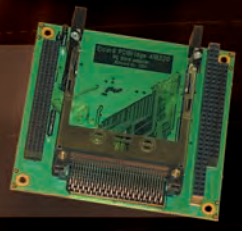

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"Ultimately, the network infrastructure has to provide support for a net-centric approach to battlefield operations. Currently, incompatibilities exist between individual weapons systems with regard to characteristics such as protocols used, bandwidth, frequencies, and media."

model for data. Such a model separates the data from its source and makes it accessible to any application running on the network; this enables the Open Architecture program to provide a data-centric environment that's amenable to expansion with new systems and applications.

Standards drive net-centricity

Standards play a key role in enabling data-driven net-centricity across all systems on a battlefield. Ultimately, the network infrastructure has to provide support for a net-centric approach to battlefield operations. Currently, incompatibilities exist between individual weapons systems with regard to characteristics such as protocols used, bandwidth, frequencies, and media. Without a common network infrastructure, systems will be unable to interoperate effectively.

A driving force behind the development of a common network infrastructure for the U.S. Navy and Air Force is the Net-Centric Enterprise Solutions for Interoperability (NESI). NESI provides guidance, best practices, and practical examples for developing net-centric software that influences the design, implementation, maintenance, evolution, and use of the Information Technology portion of net-centric solutions for military application. NESI provides – for all phases of the development of net-centric solutions – guidance that meets DoD Network-Centric Warfare goals.

From a practical standpoint, NESI drives the abstraction of individual systems data to a common data-driven environment. It marks a step toward the use of a comprehensive data bus, similar to the Enterprise Service Bus (ESB) used in the non-real-time SOA environment, that manages the flow of data between multiple weapons systems in a hard real-time networked environment.

An integrated network infrastructure

All of this leads to the infrastructure required for a fully net-centric battlefield. In such an environment, applications and application components such as Web services can be hosted on processing nodes and be able to access and use any data on the network. This requires the combination of media, protocols, and middleware to support full connectivity and data access anywhere on the network in real time.

Several efforts are underway to establish the infrastructure that meets these requirements for a battlefield network. One project that addresses this is the Common Link Integration Processing (CLIP) program. The CLIP program was implemented to develop common software and common-link processing for a joint Army-Navy-Air Force program. It allows existing platforms without a tactical data link, as well as platforms with different tactical data links, to communicate with each other.

Fully leveraging this capability is the Boeing B-1B effort. By using CLIP with a data-centric DDS interface, they can simply subscribe to "Tracks" and receive all track updates from numerous tactical data links without worry of data format, data state, failure semantics, or data source; the middleware and QoS based data-centric infrastructure manages these details.

Moving toward a comprehensive battlefield network

Despite these and other efforts, much work remains on the creation of a net-centric approach to battlefield operations. A big step in building out a data-driven network is the infrastructure for communication across the hundreds of different types of devices in a dirty and noisy environment. The infrastructure incorporates media, protocols, and middleware that enable performance and service characteristics across multiple connected systems and devices.

Beyond the network infrastructure and data communications among the multiple devices, applications using data-driven architectures must be built in order to take advantage of real-time data availability from multiple network nodes. These applications must have seamless access to data from multiple devices, reach a determination on a course of action for a single system or a set of battlefield systems, and cause the execution of that course of action through a coordinated response of weapons systems or other battlefield devices, such as GPS devices or soldier-carried computers.

It will take years for the vision of a true net-centric battlefield to emerge to reality. But the benefits will appear gradually, as the network and its components' systems are built out and deployed in the field. Data-driven applications can be written today to give battlefield commanders greater insight into operations and force deployment.

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Conquering new military network management challenges

By Carl Moberg

Photo courtesy of the U.S. Air Force by Tech. Sgt. Reynaldo Ramon

Advanced military networks require complex provisioning and can no longer be dependent upon manual administration approaches. Methods such as Command-Line Interfaces (CLIs) and Simple Network Management Protocol (SNMP) exist, but their limitations are somewhat prohibitive. Accordingly, a new approach to the problem has recently become an IETF standard called* NETCONF*, an XML-based protocol specifically designed to configure the most demanding network situations by providing automated configuration management, improved network security, robust configuration changes, and Policy-Based Network Management (PBNM).

Communications networks play an increasingly vital role in modern warfare and defense systems. Emerging network-centric operational doctrines seek to convert an information advantage into a competitive operational advantage through networking and information sharing among dispersed forces. Programs such as the U.S. Navy's Cooperative Engagement Capability (CEC), the U.S. Army's Future Combat Systems (FCS), and the U.S. Department of Defense's Transformation Satellite Communications System (TSAT) are moving to an increasingly network-centric warfare model.

This emerging paradigm creates significant challenges from a network management perspective. Military networks are larger, more diverse, and more central to mission success than ever before. Rapid force deployments and changing operations drive constant network configuration changes.

In this environment, configuration errors can easily cause network outages, and system downtime risks lives. The software that monitors, configures, and controls these networks must be designed for high performance, continuous service, ironclad security, and fast, error-free adaptation to the rapidly shifting needs of the modern mission. This is best accomplished with a standards-based architecture that provides strong security features, robust operations, and proper architectural support for rapid, error-free, automated configuration.

Current approaches such as Command-Line Interfaces and SNMP – which rely on manual configuration of individual devices or on large libraries of proprietary scripts – will fail to meet the requirements of future forces. However, the NETCONF standard, an XML-based protocol, is specifically designed to support automated configuration management and provide improved network security, robust configuration changes, and policy-based network management. These capabilities make it an elegant and efficient solution to next-generation military network management challenges.

Limitations of current approaches

As mentioned previously, different approaches exist for managing network devices, including CLI and SNMP, but each has its own limitations (see Table 1).

Approach	Configuration Challenges
Manual Configuration	Prone to human error Labor intensive, not scalable No transaction and rollback management
CLI Scripting	Maintaining scripts time consuming Device changes risk scripting errors No transaction and rollback management
SNMP	Best for monitoring Security issues No transaction and rollback management

Table 1

Traditional CLI approach

The traditional approach to managing network devices has been to use manual configuration interfaces, such as CLIs. However, using unique management interfaces for each networking device can result in a lack of consistency between devices as well as a lack of integration with other applications. Further, configuring individual devices by hand, even aided by a central management console, is not a scalable approach due to low productivity levels and the likelihood of human error.

One approach to automating network management activity is to develop CLI scripts for the devices in the network, send textual commands to each individual device, and analyze its textual output. Fresh scripts are written and tested as new equipment is added. The library of scripts comes to implicitly embody all knowledge of the network. Maintaining the scripts becomes an ongoing challenge and another opportunity to introduce human error.

To interface *ad hoc* scripts to consolidated management servers, such as Network Management Systems or Operations Support Systems, requires a "mediation layer" of adaptations. This is expensive to develop and maintain. In addition, multi-box transactions are rendered difficult by the lack of a standardized scripting model for equipment from multiple vendors and the absence of locking and other semantics needed to ensure consistency and correctness of changes across the network. A preferable method is to formalize the network architecture and network elements into a complete and cohesive data model that is used by both the management system and system administrators.

SNMP poorly suited to configuration management

While SNMP is well established and works well for monitoring network devices, it is not a good solution for configuration management. First, SNMP operates over User Datagram Protocol (UDP), an unreliable datagram protocol. Second, SNMP uses a protocol-specific security mechanism rather than a standard method, increasing administrator workload and complicating network architecture. Third, because UDP limits the maximum message size, large configurations cannot be sent in a single datagram. Finally, although some vendors provide proprietary mechanisms, SNMP lacks a standard method to allow the network to revert automatically to a working configuration in the event of a configuration error. For these reasons, SNMP is rarely used in practice for writing configurations.

IETF and automated configuration management

The IETF has acknowledged the need for an improved standard for automated network configuration. Therefore, in December 2006 an XML-based protocol called *NETCONF* was finalized (RFCs 4741-4744). Equipment vendors and network operators are taking advantage of NETCONF to facilitate scalable deployments of networks without the risks of disruptive configuration errors. Figure 1 shows the structure and layers of the NETCONF protocol.

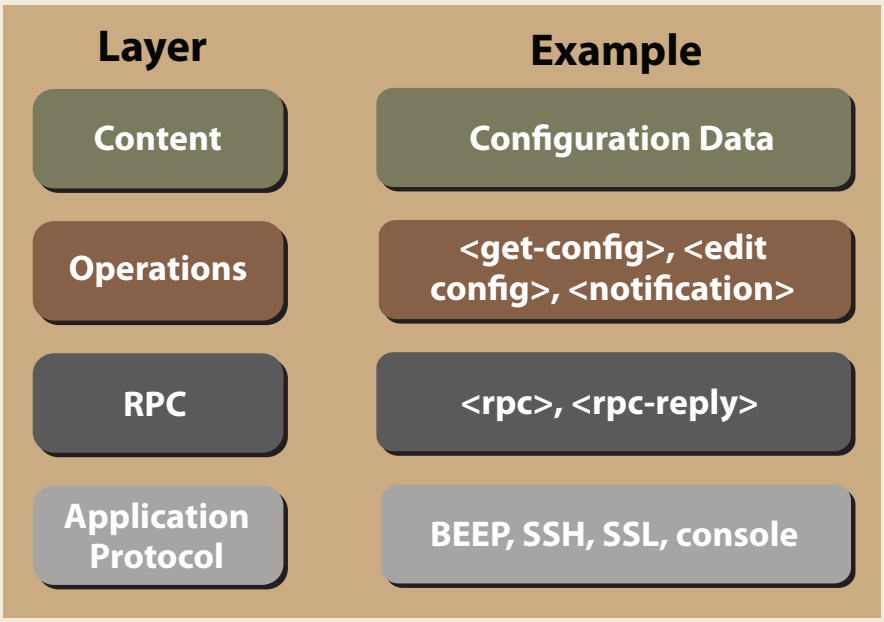

Figure 1

NETCONF offers a number of compelling features that lend themselves well to the particular requirement of next-generation military networks for a management solution that is secure, robust, facilitates a high degree of automation, and is standards-based and commercially supported.

Improved network security

NETCONF is a Remote Procedure Call (RPC)-based protocol that uses XML encoding for protocol messages and configuration data exchanged between managers and agents. XML requests and responses are sent over Secure Shell (SSH), a persistent, secure, authenticated transport protocol. Encryption ensures that the requests and responses are confidential and tamper-proof. In addition to a secure communication system, NETCONF requires devices to track client identities and enforce permissions associated with identities. This means that devices can be managed over an untrusted wide area network, a distinct advantage compared to other approaches. Configuration over a WAN has the further advantage that network management can be centralized through consolidation of all management to a single site, but also decentralized as multiple sites can share device management work.

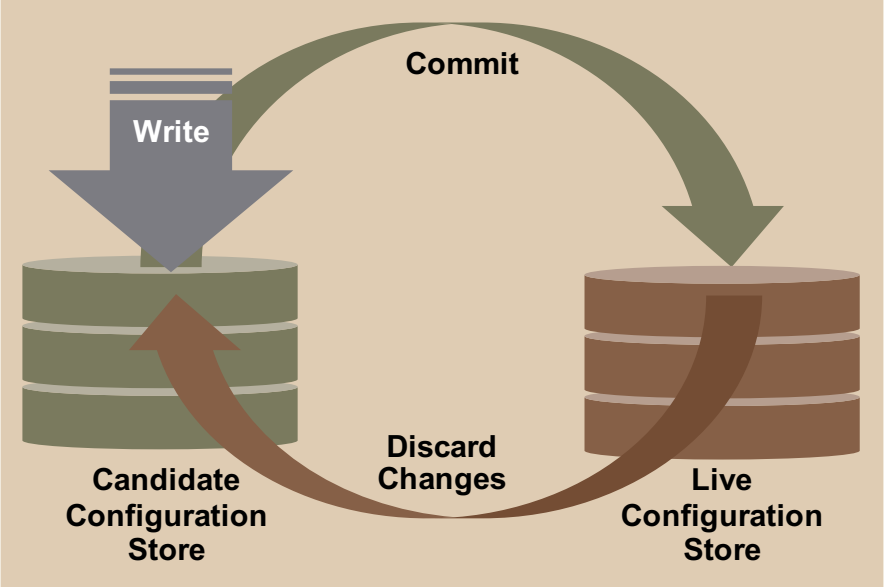

Figure 2

Robust configuration changes

NETCONF increases the robustness of dynamic networks by providing built-in safeguards to ensure that configuration changes are made in a valid and consistent manner across all network devices. As depicted in Figure 2, a configuration change will be initially written as a candidate and will only be enacted or committed if no errors occur. After a configured interval, devices automatically revert to their original configuration, unless the change has been confirmed by a second, confirming commit. Administrators can use this capability to test configurations that might potentially degrade or disable connectivity. If such an error occurs, the confirming commit does not reach the misconfigured devices and, after a timeout, the network automatically reverts to the original working configuration.

Policy-Based Network Management

NETCONF's strength in transaction management also lends itself to Policy-Based Network Management, an approach that promises to push the science of network administration to even greater levels of automation and efficiency in reacting to dynamic network conditions, but tends to trigger frequent configuration changes and

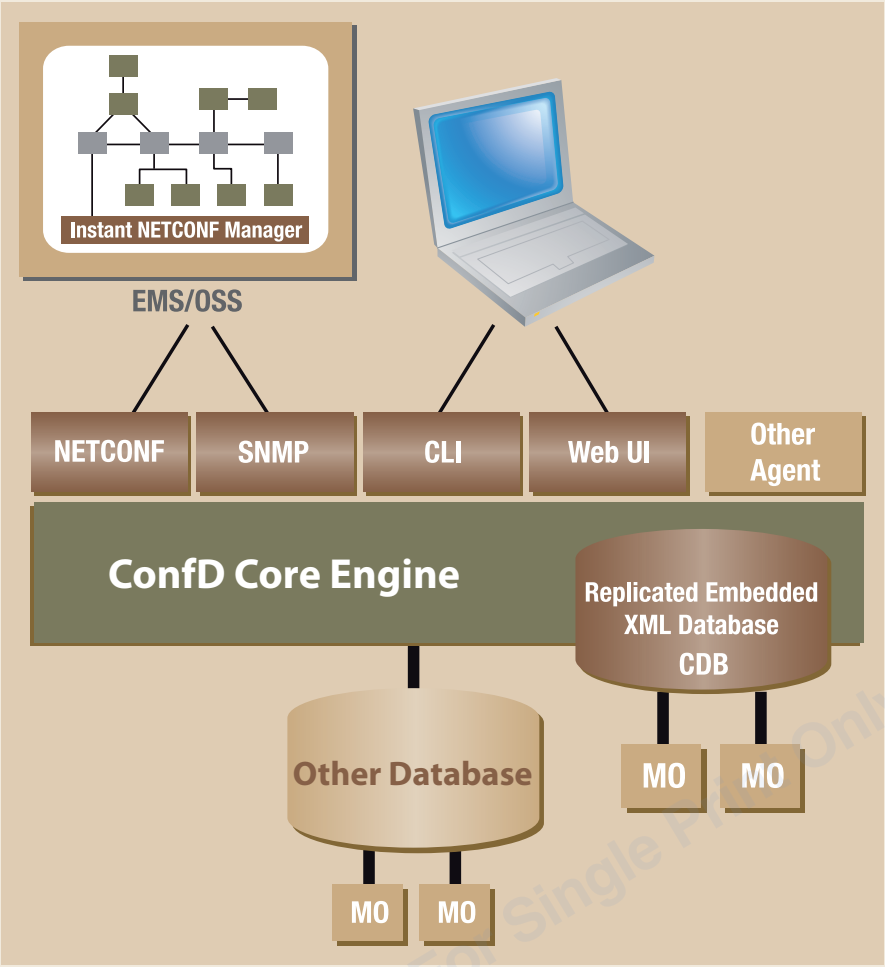

Figure 3

complex multi-step transactions. For example, NETCONF provides protocol mechanisms for locking configurations and manipulating configurations in bulk. By locking and working on multiple devices simultaneously, a management system built on NETCONF can implement network-wide policies as logical management operations.

Tail-f Systems provides XML-based network management software for enterprise-class and carrier-grade networking equipment and plays an active role in the IETF Working Group on NETCONF. Tail-f's ConfD software (see Figure 3) enables equipment suppliers to rapidly implement key management interfaces including CLI, Web UI, SNMP, and NETCONF with a robust infrastructure to meet rigorous requirements for high availability and security. ConfD implements the same transaction model used by the NETCONF standard for automated configuration management across all management interfaces.

Making the connection

Military networks are larger and more complex than ever before and are becoming increasingly mission-critical under the emerging doctrine of network-centric operations. Enter NETCONF, which supports automated configuration management and provides improved network security, robust configuration changes, and Policy-Based Network Management to help conquer the challenge.

Carl Moberg *is vice president of engineering at Tail-f Systems. Prior to joining Tail-f, he was the cofounder and director of product management at ServiceFactory. Before joining ServiceFactory, he worked at Telia, where he was one of the principal architects of the company's Internet service platform. He can be reached at carl.moberg@tail-f.com.*

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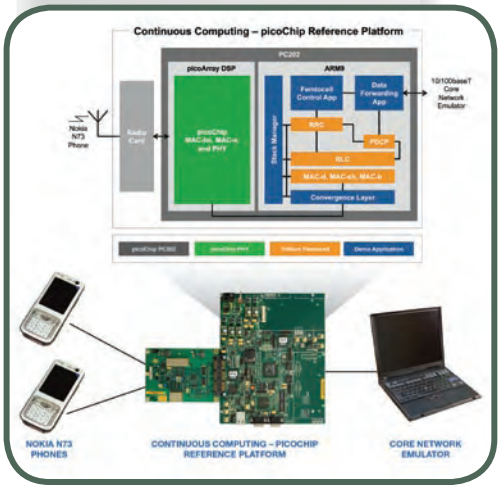
Cell phone range extender reference design

As cell phones proliferate across the civilian world, they've also found their way onto the battlefield. Not that they're standard DoD-issued items; rather, military personnel often find that mobile phones present a convenient way to communicate non-classified information in urban settings and interface to POTS lines. But surprise! The military has the same problem as the rest of us: poor reception and spotty coverage. The High-Speed Packet Access (HSPA) femtocell software reference design from Continuous Computing and picoChip aims to change that. A *femtocell* (10E-15) is basically a miniature cell phone tower/repeater/infrastructure station that drastically improves cell phone reception in spotty areas. The market for low-cost, consumer, in-home femtocells may reach $850 million by 2011 (reference: Unstrung Insider), so you know it's low-cost COTS.

Combining Continuous Computing's Trillium Femtocell protocol software with picoChip's PC8208 software and PC202 picoArray SoC, the reference design seeks to reduce project risk and complexity, while improving time-to-market. The design works with 3G/4G protocols at HSPA data rates, and the ARM-based PC202 maintains a low-memory footprint while supporting a multicore DSP fabric for running picoChip's PC8208 baseband code. Collectively, the design includes Trillium SIP and UMTS Generic Access Network (GAN) core network interface options, and is compliant to 3GPP specifications through Release 7. The reference design provides RF interface, data processing, and application processing support and can service voice, video, and high-speed wireless (cell-based) data. We don't know about you, but we want one in our office.

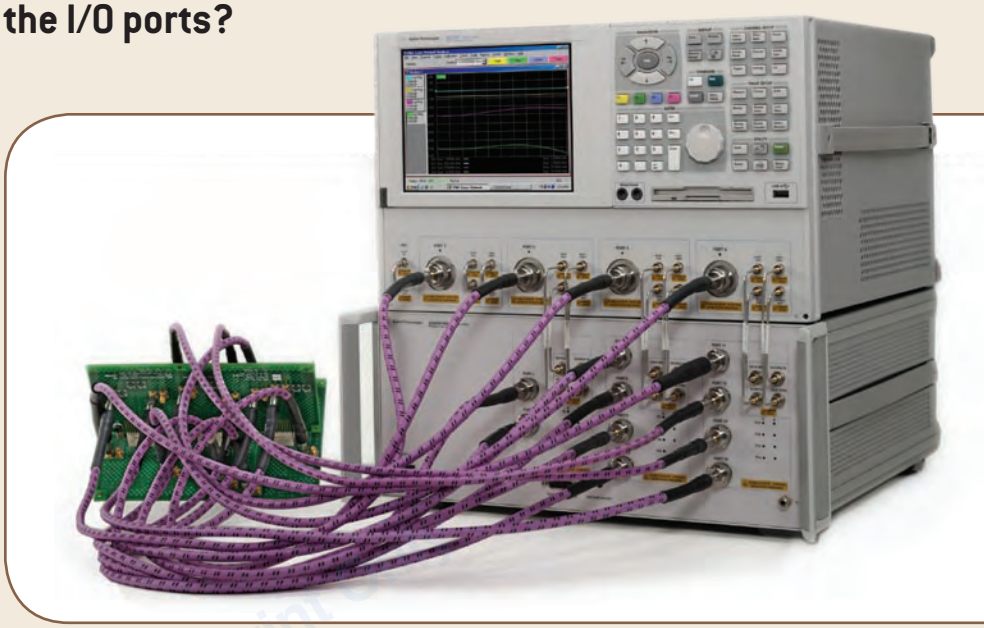
Continuous Computing
www.ccpu.com • RSC# 37428

picoChip
www.picochip.com • RSC# 37429



Denser networks, denser devices

The question is: how to test the I/O ports?



By Wayne Smith

Advanced packaging and integrated circuit manufacturing techniques have resulted in multi-port devices that are difficult to characterize using traditional two- or even four-port Vector Network Analyzers (VNAs). A new class of test set extends the capabilities of the traditional VNA to N-ports, which provides full S-Parameter characterization of multi-port devices.

Denser integration and a trend toward using balanced I/O have increased the number of I/O ports on many devices such as network switches, bridges, and fabric muxes. While the overall performance of the assembly containing an integrated circuit device may improve compared to an earlier discrete component version, the performance of the individual components inside the IC is usually less than that of corresponding discrete components – particularly with regard to isolation. As a result, it is necessary to measure the effect of each port of a multi-port device, on itself and every other port on the device. This is done by measuring the S-Parameters for each two-port pair with all other ports properly terminated or error-corrected.

This would be a daunting task for a high-count I/O device if a two-port or even a four-port VNA were used since the number of single-ended S-Parameter measurements required is N^2. For example, an eight-port device requires 64 S-Parameters to completely describe its single-ended behavior. Using an automated switch matrix would save time, but it would often degrade performance unacceptably. Manual testing could meet stringent accuracy requirements, but it would be unacceptably time consuming.

A new class of external test set that extends the port count of a VNA has evolved to meet multi-port testing needs. Commonly called *N-port network analysis,* where N is the number of ports on the device and the number of fully calibrated test ports, it uses internal switches and couplers to *seamlessly* integrate the test set with the VNA. This gives the N-port test set performance that is comparable to that of two- or four-port VNAs. Using N-port network analysis, the S-Parameters of any combination of port pairs on a multi-port device can be accurately measured with the systematic errors of all test ports and paths removed by error correction routines. Currently, 8-port and 12-port versions of N-port network analyzers are shipping, but there is no upper limit on the number of test ports that could be made available. Calibrating such an instrument would be time consuming if done conventionally, but fortunately techniques have been developed to greatly shorten the calibration process without compromising measurement quality.

N-port network analysis has obvious application in R&D where it allows designers to quickly characterize a device and import the model into a simulation program. Similarly, production engineers are beginning to use N-port network analysis as an alternative to device-dependent test in production. Multi-port devices commonly require external components on some ports in order to operate. Often, "golden" components are built into test fixtures in production, which makes all test results dependent on those external devices. Using N-port network analysis, the multi-port device is first characterized and then functionally tested in simulation using ideal external components. The Agilent N5230A based physical layer test system (pictured) provides a high-performance and cost-effective solution for differential interconnect analysis. The novel instrumentation architecture enables faster measurements with a lower noise floor, thus providing faster design cycle times.

Wayne Smith *recently retired from Agilent after 29 years of holding a variety of product planning and marketing positions. His most recent job was an aerospace/defense applications engineer in the Wireless Business Unit at Agilent Technologies where he focused on cellular technologies. For the past 11 years, that work has been exclusively focused in the area of RF and microwave products for the cellular and aerospace/defense market segments. Wayne graduated from the University of Nebraska in Lincoln with a Bachelor of Science in Education. For more information on this article, please contact John Barfuss at john_barfuss@agilent.com.*

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Editor's Choice Products

New Java tool for your workbench

Java is emerging as an extremely efficient, rigorous, and low-footprint way to talk to hardware – especially in real-time, deterministic systems. Moreover, the emerging JSR-302 safety-critical version of Java tightens up the code even more by providing assurance and guaranteed performance timing (and control over garbage collection!). So it's a natural that these benefits, when needed, should be bolted up to the most popular RTOS in military applications: VxWorks. And sort of like that beloved Reese's "chocolate/peanut butter" commercial, Aonix and Wind River Systems are all giggly with their newfound software marriage.

Aonix's PERC Pico 1.1, which is based upon the emerging JSR-302 spec, allows developers to write deeply embedded code for resource-constrained hard real-time systems. Code constructs include device drivers, interrupt handlers, control plane communications, and even multimedia signal processing inner loops. The "hundreds of kilobytes" footprint (per Aonix) is easy on your system, while maintaining the modularity and portability essential for long-life military programs. When bolted to VxWorks, and facilitated through Eclipse plug-ins via Wind River's Workbench development tool, designers can cover the full software stack: from "bare metal" all the way up to application code.

Aonix • www.aonix.com • RSC# 37426

More FPGAs power VPX DSP board

As FPGAs trounce the world of DSP designs, having more of them – with more I/O and more memory – is "more better." Curtiss-Wright Controls Embedded Computing's CHAMP-FX2 – the latest incarnation of the company's venerable CHAMP DSP series – uses two Xilinx Virtex-5 LXT FPGAs to provide true heterogeneous processing. A "lowly" Freescale 8641D PowerPC processor handles general purpose processing, as well as DSP algorithms in its own right. Collectively, these three nodes are mounted on a 6U VPX board that affords more I/O capabilities than Bill Gates has copies of Windows. Well, maybe not that many, but a lot.

Each FPGA node is swimming in memory: up to 1 GB DDR2 SDRAM (4.4 GBps peak), and up to 32 MB QDR-II+ SRAM (8.8 GBps peak). Additionally, nodes are interconnected in various ways: four-lane RocketIO LVDS; four-lane high-speed serial links to the backplane, XMC site, and one optionally to the front panel; and 18 pairs of discrete LVDS to the VPX-equipped backplane in case you want to roll your own. And the 8641D *dual core* is no slouch either. It can run up to 1.33 GHz, has up to 1 GB of DDR2 SDRAM with ECC, and 512 MB of flash plus 128 KB of NVRAM. There's Ethernet (2), serial (2), and an onboard Serial RapidIO switch spidering lines all over the board and out to the VPX backplane. There's more, but we're out of room. Check it out at the Curtiss-Wright website.

Curtiss-Wright Controls Embedded Computing • www.cwcembedded.com • RSC# 34875

Brightness beyond "nits"

By now everyone knows that regular, everyday laptops are used by our war fighters on the battlefield, in command centers, on ships, and even in the International Space Station. But what's not so obvious is that a plain vanilla COTS laptop isn't ideal in dirty, rugged, and full-sunlight situations because they just won't survive. A better solution is a "semi-rugged" laptop from a company that's been there before – someone like General Dynamics Itronix. After all, you'd trust the same company that makes the Army's main battle tank, wouldn't you? Itronix's VR-2 notebook is as current as you'd find in any office supply or electronics store, *and it is designed for rugged duty*. But most importantly – its patent-pending screen is sunlight readable in the real world.

The 13.3" DynaVue screen doesn't just crank up the backlight for brightness; it optimizes the contrast ratio while minimizing glare and reflection. The result is a Core 2 Duo (T7300, 2.0 GHz) machine with integrated graphics that weighs the same or less as most business laptops: a mere 6.2 lbs. But this one can withstand 26 drops from 30 inches, has an integrated five-band antenna for worldwide wireless coverage (depending upon the installed radio), Bluetooth, and 802.11 a/b/n Wi-Fi. And since it's from General Dynamics Itronix, security is top-notch, with a TPM 1.2 module, stealth mode, "super password," BIOS password, and optional biometric fingerprint reader. Various hard mounts are also available to work in vehicles or other rugged applications.

General Dynamics Itronix • www.gd-itronix.com • RSC# 37431

Fanless, wireless, but *not* brainless

With some embedded products, saving SWaP and cost means living with anemic performance from low-end microcontrollers. But the NTC100-LX800 from Advansus is designed for high-quality multimedia data streams up to a 500 MHz clock rate. Advansus – a joint venture between ASUS and Advantech – specializes in value-add services. The company created this little Nano-ITX based box to solve multimedia problems in wireless security and remote monitoring applications.

The svelte 170 mm x 155 mm x 42 mm box is based upon the AMD Geode LX800, which, with its combination chipset, together sip a mere 2.5 W. Power is supplied via a 12 V source, and no fan is required to keep the box cool in most environments. I/O includes a Mini-PCI slot (for the radio/antenna), 24-bit TTL, 18-bit LVDS, AC97 audio, Ethernet, four USB ports, CompactFlash, and an internal HDD. There is additional room inside the chassis for optional add-on boards, making the NTC100-LX800 ideal for custom COTS-based military and homeland defense applications.

Advansus • www.advansus.com • RSC# 37432

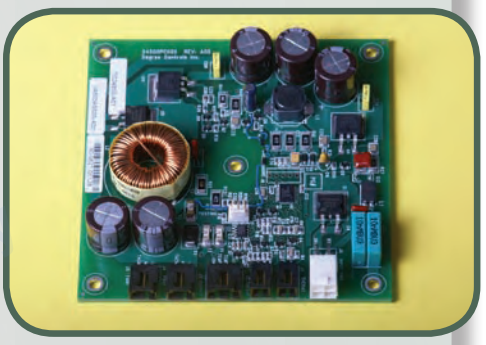
Small, extended temp resolver converter

Electromechanical systems and sensors most often have "spinny things," where knowing precise, angular information and speed is critical. Tachometers, encoders, and resolvers are among the most common types of rotational sensors – but getting their outputs into the digital realm requires conversion. In particular, a resolver-to-digital converter needs sufficient resolution, phase measurement, and even operation over a wide temperature range. These characteristics all describe the RD-19240FS-100 R-to-D converter family from DDC-I. Available in a small 64-pin LPCC (9 mm) or 52-pin MQFP (100 mm) package operating over -55 °C to +125 °C, the 19240 Series is also designed for low cost.

Programmable versions offer 10-, 12-, and 14-bit resolution, and resolution is highly repeatable to 1 LSB in 14-bit mode. Dynamic configurability is also handled via programmable dual-bandwidth output and tracking rate, and a BIT output can monitor for loss of signal, reference frequency, or tracking. Nominal supply voltage is ±5 VDC with an accuracy up to 8 arc-minutes, and an internal synthesized reference can provide up to to a very wide 45-degree phase shift correction. If you've got a "spinny" sensor, resolve to give the 19240 family a look.

Data Device Corporation • www.ddc-web.com • RSC# 37433

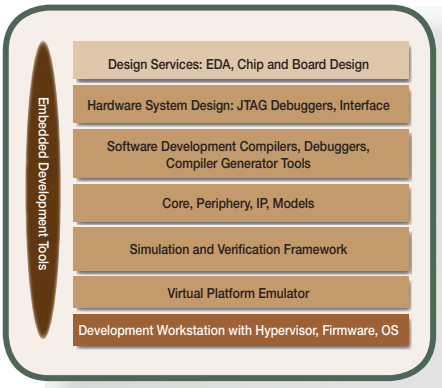
MIL-STD-461 fan controller



Not all military systems are conduction cooled; in fact, most of the systems used in defense applications are convection cooled and often use fans. But have you ever stood next to a cage with 10,000 RPM fans screaming at full throttle? The best solution is to manage those fans with an intelligent controller that can also serve in rugged applications. Such is the case with Degree Controls' rugged military fan controllers, which meet both MIL-STD-461 for EMI/EMC and MIL-STD-810F for environmental constraints.

The family of products utilizes microcontroller designs and DegreeC software to monitor system temperatures and adjust fan speed(s) accordingly. Programmable alarm thresholds can be set, along with speed curves that more precisely adjust temperatures to minimize thermal shock or deal with specialized ambient conditions. But beyond just a robust feature set, what sets DegreeC's products apart is the company itself: a Cage Code (when was the last time you read *that* term?), ITAR registered, and rigorous test methodologies including HASS, HALT, ESS, MTBF, and all the "ilities" you'd expect from a MIL-SPEC supplier. The company also provides specialized heat sink designs, as well as thermal and airflow sensors.

Degree Controls • www.degreec.com • RSC# 37434



Power.org's tools trio

Thinking of using a CPU, chipset, or other device that conforms to the Power Architecture? If so, you're going to be a happy camper when you feast your eyes on three new tools from the Power.org organization: Solutions Portal; the Power Architecture Early Tools Development Matrix; and the Power.org Target Debug Capabilities Specification. We've bestowed upon this set of information tools an *Editor's Choice* award because it eases design efforts for the ever-popular Power Architecture. Collectively, the tools are designed to save you time, provide access to resources, and enhance interoperability and architecture compliance. First up, the *Portal* is a one-stop repository for all things Power: tools, software, hardware, and services. Architects and designers should "shop" here first for information, and vendors should make sure their products are up to date (www.power.org/solutions).

The *Early Tools Development Matrix* (see graphic) demonstrates the breadth and depth of development tools available for Power Architecture cores and SoCs. More than a pretty face, the matrix is a categorized and comprehensive listing of available tools. Finally, the *Target Debug Capabilities Specification* defines a common set of debugging requirements for Power-based products. The spec, which is an extension of the Power Instruction Set Architecture, includes required and recommended functions, environments, and debug features. Sort of a no-brainer, the spec brings uniformity and interoperability to the large and growing Power ecosystem.

Power.org • www.power.org • RSC# 37427

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New Products

By Cliff Witte

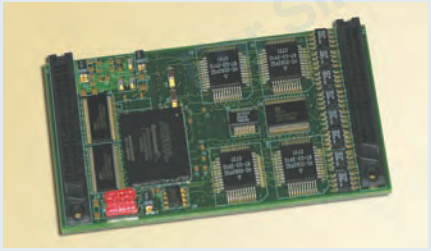
INDUSTRIAL GRADE TABLET COMPUTER

Advantech Corporation
Website: www.advantech.com/applied
Model: 10.4" Industrial Tablet PC **RSC No:** 36505

A 10.4" industrial-grade tablet computer with a fanless design • Supports ULV Intel Core Duo U2500 1.2 GHz processor • IP54-rated, fully sealed chassis for water/dust resistance • Rugged design protects system from shock/vibration damage • Powerful communication capabilities with optional built-in WLAN, Bluetooth, and GSM/GPRS/EDGE modules • Supports Windows XP for easy development • Wide -20 °C to +55 °C operation for extreme environments

AVIONICS SERIAL BUS INTERFACE

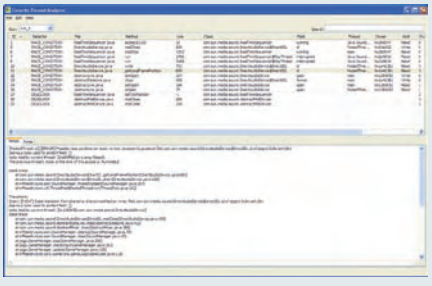
ALPHI Technology Corp.
Website: www.alphitech.com
Model: IP-ARINC 429 **RSC No:** 37178



A high-density IP module interface for avionics protocols • 16 independent receiver channels • Eight independent transmitter channels • Label matching for all receiver channels • Eight x16 bits A/D channels • One 64 Kword SRAMs buffer for storing data • Burst and continuous mode for transmitting data at the rate of 100 ms to 1,200 ms • 8/32 MHz IP clock

THREAD ANALYSIS TOOL

Coverity
Website: www.coverity.com
Model: Thread Analyzer **RSC No:** 37020



Dynamic analysis tool for multi-threaded applications • Automatically detects concurrency defects that can cause data corruption and crashes • Unique thread analysis automatically detects concurrency defects including race conditions and deadlocks • Sophisticated technology allows the tool to run with a significantly lower impact on memory and system performance than similar tools • Immediately find and correct concurrency defects in order to accelerate overall software development • Static and dynamic analysis products can be connected to create a powerful combination for ensuring high-quality software

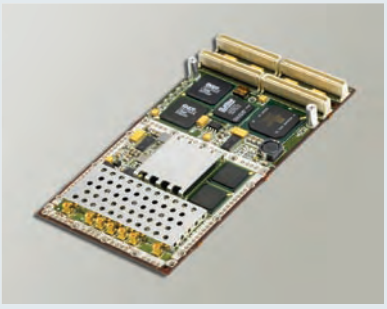
IPMI MANAGEMENT SOFTWARE

Emerson Network Power
Website: www.emersonnetworkpower.com/embeddedcomputing
Model: SpiderwareM3 **RSC No:** 37207

Platform management software designed for remote management, monitoring, and maintenance of multiple IPMI-compatible platforms • Automated acquisition and update of IPMI information from AMC modules and platforms • Intelligent alarm monitoring and prioritization • Fault and alarm alerts • Sensor threshold setting • Monitoring of CPU and memory usage • Temperature monitoring and threshold setting • Field-replaceable unit information • HPI and XML over TCP/IP interfaces • DHCP configuration management

RUGGED ADC PMC MODULE

GE Fanuc Intelligent Platforms, Inc.
Website: www.gefanuc.com/embedded
Model: ICS-8554B **RSC No:** 36713



A rugged four-channel 105 MHz ADC PMC module with DDCs, Xilinx FPGA, and PCI 64/66 interface • Four transformer-coupled ADC channels: 14-bits @ 105 MHz • 2 GrayChip GC4016 DDC ASICs • 3M gate Xilinx Virtex-II FPGA • 66 MHz, 64-bit PCI 2.2 DMA interface • 2 MB FIFO buffer • Pn4 user I/O supports LVTTL or LVDS signaling levels • Internal or external clock and trigger • > 67 dB SNR and > 80 dB SFDR • Multiple board synchronization • Extensive application and technical support available • VxWorks, Linux, and Windows device drivers

6U CONDUCTION-COOLED ENCLOSURE

Hybricon Corp.
Website: www.hybricon.com
Model: Forced Air, Conduction-Cooled Enclosure **RSC No:** 36384

A forced air, conduction-cooled enclosure • An integral subsystem responsible for digital signal processing • Top load • 6U, 20-slot, dip brazed card cage with folded fin stock • Welded outer construction • High-powered extreme environmental fans to handle extended temperature range • Front air intake, rear exhaust • Sealed card cage to protect against foreign matter • Custom backplane using RF feed through connectors • Integrated RF wiring • Will accept multiple 400 W conduction-cooled power supplies • Front I/O panel • Chassis finished per MIL-DTL-64159 • Rugged, hinged chassis slides designed for chassis rotation while in shelter • Filtered power input via 38999 connector • 24 V DC input

.NET MESSAGING MIDDLEWARE

Real-Time Innovations
Website: www.rti.com
Model: Low-Latency Messaging Middleware **RSC No:** 37413

Ultra low-latency messaging middleware that now features support for Microsoft .NET Framework • Off-the-shelf, standards-compliant alternative to the development of custom messaging middleware • Inter-application messaging latency of less than 100 microseconds • Each application thread can send or receive up to 1,000,000 messages per second • .NET applications written in the C# and C++/CLI programming languages can seamlessly communicate with C, C++, Java, and Ada applications running natively on Windows, Linux, UNIX, and embedded real-time operating systems • Automatically converts native data representations between 32 bits and 64 bits into the appropriate format for each application

SOLID-STATE DRIVE RAID ADAPTER

Lauron Technology
Website: www.laurontech.com
Model: LT-PCI-CF **RSC No:** 37245

A high-performance PCI 64-bit, 66 MHz, four-channel SSD RAID adapter supporting data rates of up to 533 MBps • Single-slot SSD adapter • MTBF greater than 1,000,000 hours with built-in EDC/ECC and wear-leveling algorithms • Erase/Write cycles greater than 1,000,000 • Striping modes transfer data to all four channels simultaneously while mirror modes transfer data on both channels • Supports RAID 0, RAID 1, RAID 0+1, RAID 5, or JBOD • Single card solution for nonrotating media requirements • Ships with Windows and Linux device drivers along with RAID management utilities

PXI XJTAG MODULE

XJTAG
Website: www.xjtag.com
Model: XJTAG 3U PXI module **RSC No:** 37199

A 3U PXI XJTAG module • Provides a high-speed interface to the boundary scan chain • Enhanced boundary scan software to improve integration with NI LabVIEW graphical programming environment • PXI card will enable users of PXI chassis to leverage ability to debug, test, and program complex Ball Grid Array (BGA) populated printed circuit boards and systems from within an integrated PXI test platform • PXI system users also running NI LabVIEW software get the added advantage of a full set of Virtual Instruments (VIs) to interface to the XJTAG system

ULTRA-COMPACT COMPUTER

Mercury Computer Systems, Inc.
Website: www.mc.com
Model: PowerBlock 50 **RSC No:** 37147

A high-performance, ultra-compact embedded computer designed for maximum performance in minimal size • Optimized for R-T image, sensor, and signal processing in harsh environments • Fully integrated and ruggedized system that represents a new level of size, weight, and power characteristics • Unprecedented computing power next to sensors in small imaging platforms • Delivers over 100 GFLOPS of processing power • Fully configured system weighs under 7 lbs and measures approximately 4" x 5" x 6" • PowerBlock 50 Engineering Development Kit is a complete software development platform for the PowerBlock 50

OPEN DEVELOPMENT PLATFORM

Presagis
Website: www.presagis.com
Model: Aeria **RSC No:** 37415

An open, scalable, and reusable COTS software platform for the development of land, air, and sea applications • Includes Creator, Terra Vista, STAGE, VAPS XT, and Vega Prime software • Complete interoperability between development phases • Ensures reusability across multiple projects • Create high-resolution synthetic environment databases by importing virtually any GIS data, sensor materials, 3D models, and existing databases • Create and control intelligent entities, add photorealistic graphical interfaces, and interact with other simulations in a distributed environment • Develop and deploy high-performance visual simulation applications and real-time 60 Hz image generators while supporting operation on multiple hardware/operating system platforms • Track key performance parameters with accurate monitoring and collection of data for after-action reviews

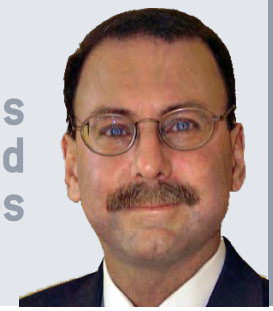
SCALABLE VME ENCLOSURE

SprayCool
Website: www.spraycool.com
Model: MPE Enclosure **RSC No:** 36991

Scalable VME "direct spray" enclosure that accepts a broad variety of electronics cards, including commercial grade and custom, with minimal modification prior to deployment • 4-21 slots for 6U x 160 mm VME, VPX, VXS, CompactPCI, or CompactPCI Express (EXP.0) electronics • 20-500 W per slot with optional MIL-STD-704 power • Capable of accepting any electronics card • Configurable I/O panel, power supply • Tested to MIL-STD-810, MIL-STD-461 • Altitudes of up to 70,000+ ft and capable of operating in temperatures of -65 °C to +71 °C • Capable of increasing densification of electronics by 4x over traditional cooling options

For more information
Enter the product's RSC# at www.mil-embedded.com/rsc

Virtualization yields hardware optimization and new embedded architectures



By Chris A. Ciufo, Editor

I've written in this space many times about multicore processors, serial switched fabrics, and virtual environments. But for the years I've been pontificating, I've always assumed that each stood on its own merits – that Freescale 8641D multicore CPUs, for instance, would add more performance to an embedded system. Or that a serial switched fabric such as RapidIO would increase the data bandwidth within a system's interconnect. Or that a virtual environment from Wind River would provide a secure partition so that multiple operating systems could be run on the same machine.

All are true, of course. But a series of very recent desktop PC and enterprise server virtualization announcements has made me wonder how the embedded space is going to react to the combination of some new COTS technologies. You might've missed these announcements; I very nearly did. (Some embedded board vendors are going to have to rethink their architectures – and even their CPU choice.) But connecting the dots between the following announcements paints a picture of radical architectural change when overlaid onto the embedded markets:

- Altera's "DO-254 Global Partner Network" and "DO-254-Certifiable Nios II Embedded Processor"
- TenAsys' "Embedded Virtual Machine eVM"
- PCI-SIG's "MR-IOV"
- NextIO's "ExpressConnect" and "nControl"

Let's get right to it, shall we? DO-254 is the hardware analog of the RTCA/FAA's DO-178B avionics software spec. DO-254 essentially says that instead of running System Function A on a dedicated but separate system from System Function B, they can be combined on the *same hardware* as long as certain hardware provisions and certification steps are achieved. This has the effect of huge savings in Size, Weight, and Power (SWaP) because one piece of hardware – processors, memory, I/O, subsystems – can safely perform multiple functions. This is sort of like brute-force virtualization, but it's a watershed in defense systems looking to save SWaP and cost. FPGA heavyweight Altera has embraced this concept with a vengeance by making their soft-core Nios II processor certifiable, along with myriad pieces of IP for their FPGAs. And voila – one FPGA can now *safely with assurance* replace entire boards in defense systems.

Virtualization vendor TenAsys has also amped up their embedded campaign through the introduction of eVM, which now allows just about any RTOS to coincide with Windows (32-bit Windows 2000 on up), and not just with the company's own INTime RTOS but with many guest OSs. For now, the hypervisor runs on a Windows OS host with multicore Intel CPUs, takes advantage of all of those Intel VT-x hardware hooks in existence, and intentionally closely couples the two virtual operating environments. The significance here is again SWaP – using one host to act like multiple machines – but there's so much more than meets the eye. In military systems, this means that any old operating system environment can be ported to work with Windows, and that includes all those old mil-specific I/O sensors that have been out of production since the 1970s. This minimizes the effort of creating virtual device drivers, keeps performance to a maximum due to data passing between OSs, and is specifically architected for determinism in real-time, deployed systems. This will get even faster when Intel multicore CPUs and chipsets implement VT-d (VT for directed I/O) to relocate bus master DMA devices[1].

And since virtualization really shines when the IC hardware is designed for it, more chipsets and I/O devices (Ethernet, SATA, graphics, PCIe, and so on) are adding provisions. The PCI-SIG just finished their Suite of Specifications, announcing Multi-Root I/O Virtualization (MR-IOV) as we went to press. If you remember the death of PCI Express-ASI, you'll understand how MR gets it right this time by extending the PCIe root complex with a protocol that virtualizes I/O *and processor nodes* for high-end servers in the enterprise. This effectively turns PCIe into a smart, fast fabric (albeit in the traditional PCI vines approach) that puts even 10 GbE to shame in data movement. Best of all: It's built into most of the ICs you'll use in new system designs.

The company NextIO provided their IP for MR-IOV, and also just announced a series of extremely impressive server devices that rely on their own PCIe 64-lane/16-port nonblocking crossbar switch that turns PCIe effectively into a bridge and reflective memory extender. In a server architecture, for instance, what once required four OSs, four servers, and 12 I/O devices (Ethernet, Fibre Channel, and SAS) can now be *reduced to only* four OSs running on two servers and three I/O devices. Amazing. The MR-IOV spec from the PCI-SIG is implemented in their switch to maximize the loading on the more-than-capable hardware that was previously underutilized. The SWaP benefits are staggering, not just in enterprise servers and ISPs, but in similarly configured embedded architectures.

Call me whacky if you want, and maybe I'm reading the tea leaves all wrong here. But we haven't even seen the *beginning* of what COTS virtualization is going to do for us. When it hits the embedded market, there will be a virtual upheaval among the dual and quad PowerPC boards with hard-to-understand serial fabrics and odd programming models. I virtually guarantee it.

Chris A. Ciufo
Group Editorial Director
cciufo@opensystems-publishing.com

[1] Intel's Virtualization Technology (VT) roadmap is complex and evolving. Search for "Intel Virtualization Technology processor virtualization extensions" and you'll find a hugely useful PDF.

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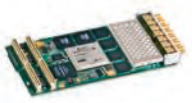

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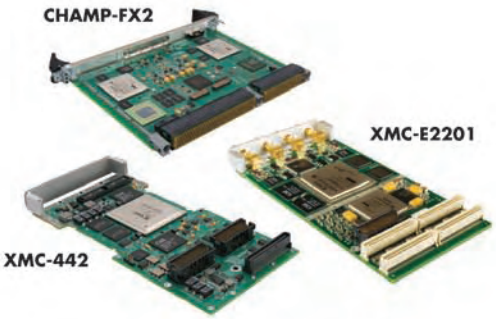

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MIL/COTS DIGEST

The Defense Electronic Product Source

July/August 2008

In This Issue

VME and **Critical Systems**

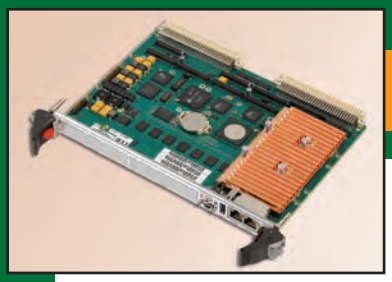
All things VME – including VPX, PMC, and system-level products ...

This special *MIL/COTS DIGEST* (MCD) supplement is dedicated to the military's VME ecosystem. Invented more than 25 years ago, VME is the *de facto* standard for deployed, open standard, high rel COTS modules. But there's more to an ecosystem than just the VME modules themselves.

Inside you'll find 25 new products that I've specially selected based upon their merit for defense applications, programs, and development systems. You'll find a healthy dose of single board computers on 6U, 3U, PrPMC, VPX, and VXS formats. In fact, the number of VXS and VPX new products is steadily increasing every month. I've also selected several mezzanine cards – in PMC, XMC, PrPMC, and the new FMC (for FPGAs) sizes. And while the commercial market for embedded chooses Intel CPUs at an ever-faster rate, PowerPCs from Freescale and IBM continue to dominate the defense market. I've included a few of them here, too. Finally, you'll find some test equipment products, middleware and software, and even an industrial grade touch screen LCD that intrigued me.

Lastly, this month's MCD supplement also contains articles from Mercury Computer Systems, VIA Technologies, Sealevel Systems, and Elma Electronic. Of course, they all deal either with VME or mission-critical systems.

Chris A. Ciufo, Editor
cciufo@opensystems-publishing.com



Dual core VME board

The MVME7100 is a VME board featuring a dual core PowerPC processor and 2eSST high-speed VMEbus interface. The board is designed to enable industrial, medical, and defense/aerospace OEMs to add performance while providing backwards compatibility. It also provides optimal speed, which is achieved due to the independence of the PCI buses for each PMC site. The board's nonvolatile memory feature prevents system memory loss in the event of a power loss. The MVME7100 is based on the System-on-Chip Freescale MPC8641D with dual PowerPC e600 processor cores, high-capacity DDR2 memory, up to 8 GB of NAND flash, PCI-X, and USB. The MVME7100 features dual integrated memory controllers, DMA engine, PCI Express interface, GbE, and local I/O. The board also supports packages for VxWorks and Linux.

www.emersonembeddedcomputing.com
EMERSON EMBEDDED COMPUTING

5-slot high-power portable tower

The Cool-M chassis is a five-slot high-power portable tower for 3U cards for military, defense, and aerospace/defense applications. It provides high-quality construction in a lightweight portable design cooling up to 100 W per slot for high-power VITA 1.7 VME64x, VXS, and CompactPCI switch fabric boards. Features include IEEE 1101.10/11-compliant card cage with Pac-2000 modular design and up to 350 W embedded power advanced cooling design (airflow: lower front to upper rear 15 CFM average). In addition, a fan mounted in rear cooling provides 130 W per slot or 65 W per slot with high-pressure PMC mezzanines. Cool-M includes peripheral mounting for front-access 5.25". It also features a CD or DVD drive and a 3.5" hard disk drive.

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Safety-critical development tool

The SCADE Suite is a certified model-based development tool for mission- and safety-critical software in aerospace and defense applications. It shortens time-to-certification with automatic code generation, documentation generation, and qualification kits to help eliminate coding errors. The SCADE Suite is DO-178B qualified up to level A. The suite provides overall model-based software development support, from requirements to target. Additionally, rigorous semantics of modeling, proven code generation algorithms, and formal proof technology are wrapped in a user-friendly tool.

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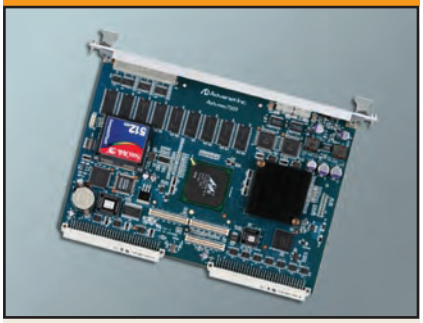
PCI Express XMC I/O module

The X3-25M is an XMC I/O module featuring two 16-bit, 130 MSps A/D channels and two 16-bit, 50 MSps DAC channels designed for high-speed stimulus-response, ultrasound, and servo control applications. Flexible trigger methods include counted frames, software triggering, and external triggering. Data acquisition control, signal processing, buffering, and system interface functions are implemented in a Xilinx Spartan 3A DSP, 1.8 M gate FPGA device. The two 1Mx16 memory devices are used for data buffering and FPGA computing memory. The PCI Express interface supports continuous data rates up to 180 MBps between the module and the host. A flexible data packet system implemented over the PCI Express interface provides high data rates to the host that is readily expandable for custom applications.

www.innovative-dsp.com

INNOVATIVE INTEGRATION

Single-slot 6U VME board



The Advme7509 is a single-slot 6U VME board utilizing a PowerPC750FX processor. The board can be used as a system controller to meet high-performance system requirements. The front panel includes two channels of 10/100BASE-TX Ethernet ports and four channels of RS-232 serial ports. A variety of memory, including SDRAM (up to 512 MB), CompactFlash, FlashROM, SRAM, and EEPROM are available. The external VMEbus is accessible via the onboard "NARUTO II" PCI-VME bridge.

www.eurotech.com

EUROTECH GROUP

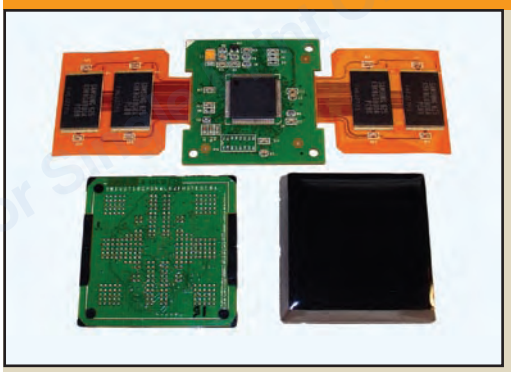
Industrial grade LCD monitor

The TuffTouch is an industrial grade, rugged 17" all-steel-enclosed touch screen LCD monitor designed for industrial and commercial environments. The NEMA 4/IP 66 LCD front panel withstands water, dust, and dirt intrusion. The high-precision, metal encapsulated viewable display is capable of running resolutions up to its native mode of 1,280 x 1,024 pixels with both analog and digital input sources. The TuffTouch has low power consumption, wide viewing angles, and superior image quality with 250 nits of brightness, 8 ms response time, and a contrast ratio of 500:1. The LCD monitor is available with resistive and capacitive touch screen options and a wide range of mounting options such as wall, benchtop, pendant arm, and ceiling mounts. TuffTouch is plug-and-play capable, requiring no video drivers or special interface cards.

www.stealthcomputer.com

STEALTH COMPUTER

Solid-state drive



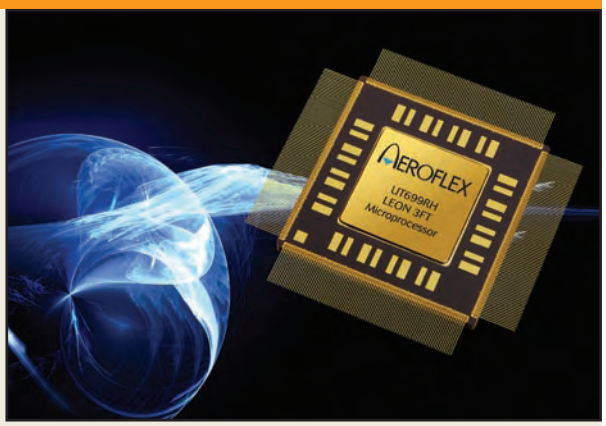
Trident's BGADrive is a solid-state drive in a standard BGA form factor that can be reflowed directly onto a PCB. The BGADrive is highly rugged for extreme environmental conditions such as military and industrial embedded systems. The BGA form factor is 29 mm x 29 mm and less than 7 mm high. It includes capacities up to 32 GB using SLC NAND flash, standard IDE, and SATA interface. Operates at extended temperatures of -40 °C to 85 °C. Custom sizes and form factors are available.

www.tridentsd.com

TRIDENT SPACE AND DEFENSE

Fault-tolerant based microprocessor

The UT699RH LEON is a 3FT-based microprocessor. Designed with Gaisler Research AB GRLIB IP-proven architecture, the LEON 3FT provides a 32-bit master/target PCI interface, while the AMBA bus interconnects a peripheral-rich environment including CAN, SpaceWire, UART, and Ethernet. The UT699RH features a power-saving 2.5 V core and static design capable of operating from 1 to 75 MHz and delivers 60 MIPS performance at 75 MHz. It is packaged in a 352-pin ceramic quad flatpack weighing 31.5 grams. The UT699FP-EVB 32-bit/33 MHz CompactPCI evaluation board is available to aid designers in system-level development.



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VXS and VPX: Cooling these hot (literally) new architectures in ATRs

By Justin Moll

The Air Transport Rack (ATR), aka* Austin Trumbull Radio*, has been the packaging format of choice for commercial and military avionics platforms. Although the mechanical configuration of the ATR has remained essentially unchanged throughout its long operational life, manufacturers have had to respond to the challenges raised by the ever-increasing power requirements of the boards installed in the units. The higher power levels of VXS, VPX, and other cards means more heat buildup in the enclosure, which presents a challenge for the packaging design. Conduction and liquid cooling solutions are available to handle this dilemma, each providing its own strengths and limitations.

Architectures such as VXS and VPX use more power and run hotter than legacy buses like VME and CompactPCI. VXS cards often run at 80 W to 100 W per slot, while VPX cards are typically 100 W to 150 W per slot. In a 10-slot ATR enclosure, that is up to 1,500 W (10 x 150 W) to dissipate. The challenge is to cool the chassis, given virtually zero airflow in many ATR applications, and a finite (and fixed) amount of space.

There are various cooling methods for ATRs. Some possibilities include air, conduction, and liquid cooling or hybrids of these styles. Forced air cooling is a common method; however, in ATR applications, the environment is sometimes sealed or otherwise has little air for entry and exit. There are also issues with Electromagnetic Compatibility (EMC) and filtering in such applications, but we'll focus primarily on conduction and liquid cooling.

Conduction cooling: A good solution, with limits

Stand-alone conduction cooling is an excellent solution for many designs, particularly for high-altitude or other applications where airflow is limited. However, it alone cannot be used in all designs, as you reach the limits of heat dissipation and removal. The heat generated within the enclosure is conducted from the heat sources on the boards through to the outer surfaces of the enclosure, and the heat is then given up to the ambient air. Internal heat pipes can be used to improve the system's efficiency without introducing electromechanical moving parts. However, while it's the simplest and therefore most reliable method, conduction cooling is also the least efficient. A conduction-cooled ATR will typically be rated in excess of 50 W per slot. So, some applications may necessitate a little assistance to transfer more heat.

Liquid cooling: Finding a practical and cost-effective form

Liquid-Flow-Through (LFT) and direct spray methods are perhaps the most aggressive ways to cool a chassis. However, these methods are among the most complicated and expensive choices available. Spray cooling, whether mist or liquid, brings issues such as:

- Water buildup
- Single point-of-failure
- Costs
- Complexity
- Space required
- Mean Time to Repair (MTTR)/ Mean Time Between Failure (MTBF)

LFT, where the liquid runs directly through each module, can also be costly and complex. However, this method may be an effective choice for the most demanding thermal management applications. Theoretically, VPX cards can use 48 V at 16 A, which is 768 W per slot. Typical VPX conduction-cooled modules today are 5 V and 12 V, with wattages in the 100 to 150 W range. When VPX modules push on the higher wattage levels in certain designs, LFT may be the right way to go. But, there is another solution to cool this wattage range with a much simpler and more cost-effective solution: Liquid Heat Exchange (LHE).

LHE: A practical choice

LHE uses the sidewalls of the chassis for plumbing the liquid. An ATR, such as the one shown in Figure 1, uses a modular liquid-heat-exchange method to transfer excess heat from VXS or VPX conduction-cooled cards. This provides much more heat transfer than conduction

Figure 1

alone. As the liquid is in a fixed area (the walls), engineers do not get into a messy situation with plugging/unplugging liquid modules. The modules for this design style are the same VXS or VPX conduction-cooled ones described earlier. The side plate assembly consists of precision-machined sidewalls, fluid carrying pipes configured to avoid sharp bends, thermally conductive inserts, and clamping brackets that can quickly be replaced as a complete subassembly in the field. The LHE design supports a thermal budget of 1,500 W in a 10-slot 1 ATR size, enabling a wide range of the latest high-performance boards to run well within their operating temperature envelope. Thermal imaging, like the example shown in Figure 2, can be used to find the hotter parts of the chassis. From there, the designer can incorporate solutions to optimize the cooling.

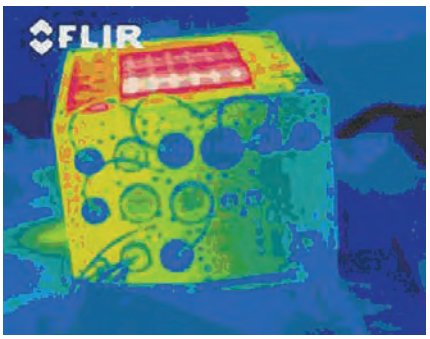


Figure 2

A dual wall modular design subassembly can also significantly reduce MTTR. The cooling sidewalls can operate as Line Replacement Units (LRUs), so a swap out is a simple process that can be carried out in the field. Each side plate has its own independent feed and return. Cooling is still provided in the event of damage to one side; the design also avoids running pipe work across the rear face of the chassis, the area most likely to be damaged if the unit is accidentally dropped. Various materials, protective coatings, and connectors can be used, enabling aviation fuel, Chlorofluorocarbons (CFCs), ammonia, or various alcohols to be implemented as the cooling fluid to suit the application. Seawater, typically at a temperature of +15° C, can also be used, which has obvious cost and availability benefits for naval applications.

It might appear strange to use kerosene as a cooling medium; however, there are significant advantages for avionics applications. The fuel is already pumped around under pressure, so a dedicated pump is not required, saving weight and space. The fuel sits at -30 °C in the fuel tanks, and therefore, it must be preheated before it can be burnt in the engine. The heat produced in the ATR, together with the waste heat from avionics and other systems, is transferred into the onboard fuel before it is fed to the main propulsion unit, reducing preheat requirements.

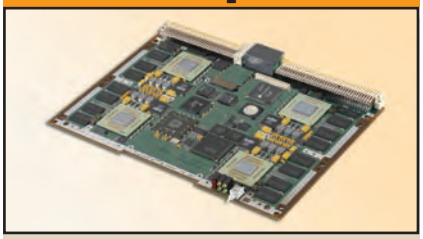
A solution found

We can tackle the thermal management challenges that new technologies such as VXS and VPX bring to avionics. Conduction cooling can solve the problem in many ATR applications, but only get us part of the way there in the higher-wattage applications. Adding LHE to dissipate heat in conjunction with conduction-cooled modules can solve the problem for many of today's applications at significantly reduced cost and complexity. ■

Justin Moll *has more than 13 years in high-tech marketing and has been with Elma Electronic Inc. since 2000. As the director of marketing experience for Elma Electronic, he has led the company's charge in several next-generation backplane and chassis technologies. Justin is active in VITA and PICMG and has been the VP of marketing for the StarFabric Trade Association. Justin received his Bachelor of Science degree in Business Administration from the University of California, Riverside. He can be reached at Justin.Moll@elmabustronic.com.*

Elma Electronic Inc.
510-656-3400
www.elma.com

6U VXS quad multicomputer

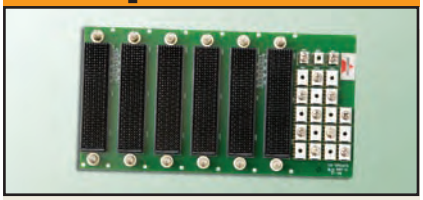


The DSP220 is a 6U VXS (VITA 41.2) quad 8641/8641D multicomputer. Featuring four single or dual core Freescale PowerPC 8641 System-on-Chip nodes, the DSP220 also has a VITA 42.2-compliant XMC slot. The multicomputer is available in six ruggedization levels including air-, spray-, and conduction-cooling in extended temperatures; the computer is also resistant to shock and vibration. It is designed for a broad range of applications including land mobile, airborne fixed, and rotary wing; it is also suitable in naval surface and underwater platforms that require high-performance COTS multiprocessors. The DSP220 can be scaled up to eighty 8641 nodes per chassis for the most demanding environments.

www.gefanuc.com/embedded

GE FANUC INTELLIGENT PLATFORMS, INC.

3U VPX-REDI backplane

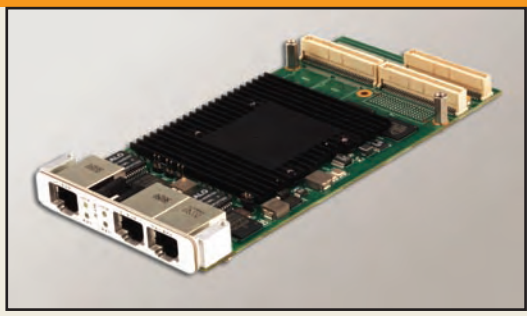


Carlo Gavazzi's six-slot 3U VPX Ruggedized Enhanced Design Implementation (REDI) backplane is designed for military and aerospace applications and ideal for deployment in harsh military environments. The VPX-REDI backplane is a COTS solution that offers high bandwidth in a compact size and integrates the latest VITA 46 and 48 standards with the proven legacy capabilities of VMEbus technology. The backplane can be customized with multiple configurations for each unique embedded development, testing, or measurement application. It is available with rear I/O, and the backplane is designed to accommodate a large volume of high-speed I/O and switch-fabric connections.

www.gavazzi-computing.com

CARLO GAVAZZI COMPUTING SOLUTIONS

PrPMC/XMC module with dual GbE



The XPedite5200 is a PrPMC/XMC module featuring the Freescale MPC8548E PowerQUICC III processor running at up to 1.333 GHz. The onboard PowerQUICC III provides integrated 64-bit PCI-X, DDR2-400/533 SDRAM, PCI Express, Serial RapidIO, and four GbE interfaces, making the XPedite5200 suitable for communications processing and general computing applications. When used as an XMC (VITA 42) module, either the 8x PCI Express or 4x Serial RapidIO interfaces can be used, in parallel or in substitution of the PCI-X interface. With software supplied by Extreme Engineering Solutions, the XPedite5200 can be installed on standard VME and CompactPCI platforms in addition to custom motherboards that support PMC sites. The module provides two GbE interfaces via the front panel and supports an additional two via the P14 backplane connector.

www.xes-inc.com

EXTREME ENGINEERING SOLUTIONS

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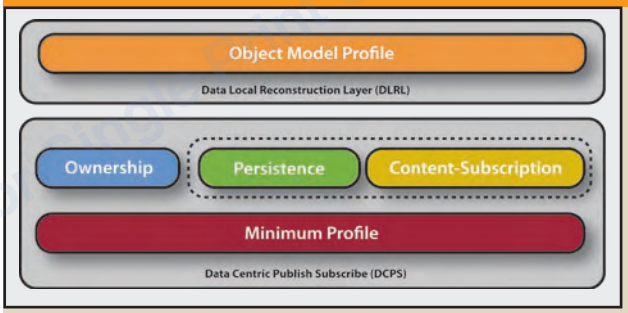

The OpenSplice Data Distribution Service (DDS) v3.2 is a real-time, data-centric publish/subscribe middleware platform. It is well suited for deployments in the most demanding mission- and business-critical distributed applications such as combat management systems, air traffic management/control, transportation, telecommunications, and manufacturing. It complies with the full profile of the OMG Data for Real-Time Systems v1.2 specification, as it provides a complete implementation of both the Data Centric Publish Subscribe (DCPS) layer and the Data Local Reconstruction Layer (DLRL) layer. It provides integration technologies with DBMS, such as Oracle, ANTS, MySQL, Web services, Real-Time Java, and CORBA. In addition, it comes with model-driven development power tools, which guide designers from system design to tuning up for final deployment.

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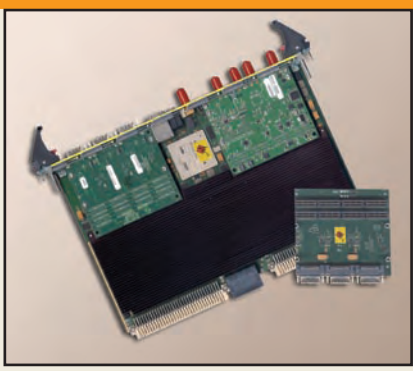

The UNI6 mezzanine card is designed to be a flexible, high-speed, multiconnector interface to Annapolis Micro Systems' WILDSTAR 4/5 main boards. The card uses industry-standard copper optical connectors and cables, which allow fast transmission of data to industry-standard devices. There are three connecters per UNI6 mezzanine card, and four full-duplex communication channels per connector. This allows each UNI6 mezzanine card to handle up to 6 GBps full duplex data rates. Interfaces that can be supported include InfiniBand, DDR InfiniBand, Rocket I/O, Aurora, Serial FPDP, and 10 GbE.

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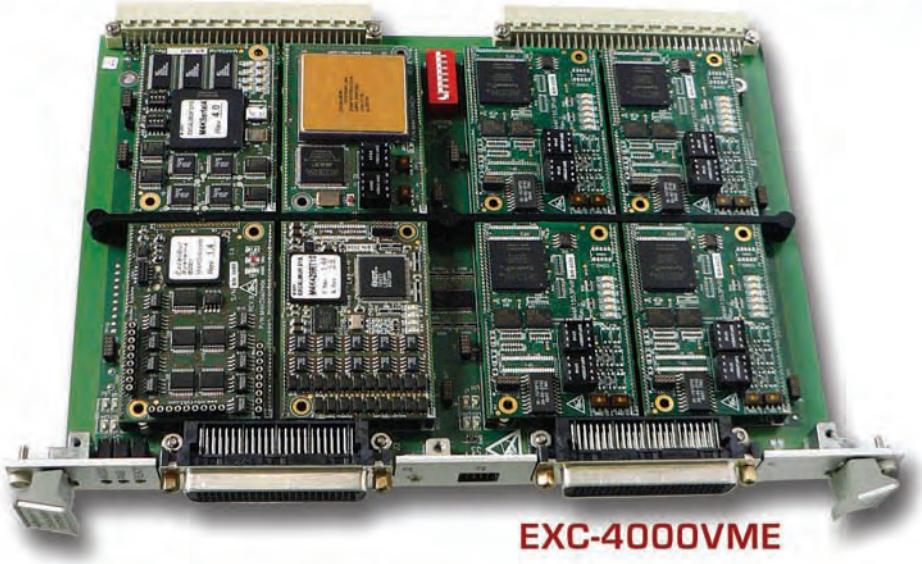

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The Little BEAR that could: The robot that saves lives

By John Lin

Sometimes war is necessary, but the cost of war is always great and many lives are lost. In an effort to diminish the loss of life, some companies have stepped up to develop robots such as the Vecna Battlefield Extraction-Assist Robot (BEAR) to rescue soldiers from dangerous venues.

In the grim reality of war, casualties are inevitable. Casualties that result in the loss of a life are tragic. But to lose a life because of inaction or neglect is even worse. Field commanders may feel the burden of a moral dilemma when extraction or rescue decisions need to be made. Should the life of a healthy soldier be risked to save the life of a wounded soldier? All life is valuable. Yet in a tactical sense, attempting an extraction or rescue may not be the most practical decision – though it is certainly an honorable one. So what should a field commander do? In the heat of the moment, decisions need to be made with clarity and level thinking – not based on emotions.

To date, more than 655,000 (all wars since 1775) U.S. service members have died in battle[1]. These numbers do not include the other 538,000+ deaths of U.S. service members that occurred in wartime. How many of those battle deaths could have been avoided remains unknown. But with the benefit of modern technology, those numbers may not have to increase too much. Wouldn't it be great if there were a robot that could save (or try to save) a human life? Movies such as "I, Robot" show how useful robots could be. In the movie, the NS4 robots sacrificed themselves without hesitation in order to prevent Del Spooner from being killed. Because robots have no emotion, there is no hesitation and no fear when it comes to executing an order. Robots that are programmed to rescue humans would make the perfect addition to military medical teams. However, such robots are thought to be only in the realm of science fiction, aren't they? Maybe, but the Battlefield Extraction-Assist Robot (BEAR) just might prove otherwise.

Meet the BEAR

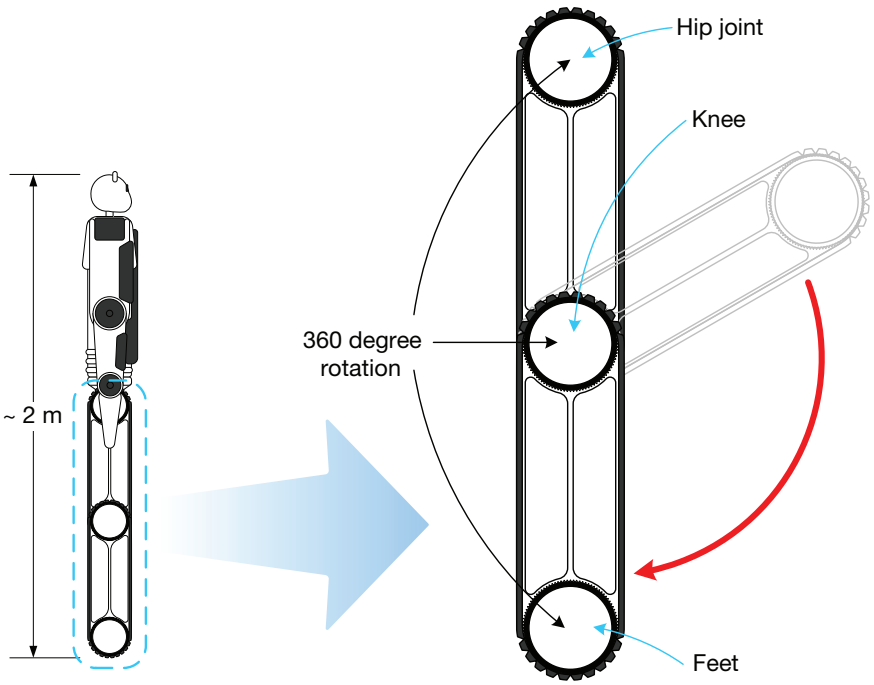
Today, more and more companies are engaging in the research, development, and production of technology that is poised to make an impact on the battlefield. One of the notable products in development is the BEAR.

A BEAR that treads lightly

The main purpose for the creation of the BEAR is reflected succinctly in the first two words of its acronym: battlefield extraction. It was intended for rescuing soldiers. And as such, it needs to be able to go where people can go. This requirement for extreme mobility meant that it would probably need legs of some sort, so its legs provide the BEAR with various methods of mobility. With its legs, the BEAR can walk, balance on any joint, and roll around using any part of its legs. Its most efficient means of mobility will be via the tracks on its legs. Using its tracks, it can traverse up and down stairs, so soldiers wounded on the upper floors of a building in an urban battlefield can rest assured that help is on the way.

The BEAR's tracks are powered by an electric motor capable of propelling it at speeds up to 10 mph. Granted, that may not sound fast, but to a wounded soldier, 10 mph is better than 0 mph. For rescue purposes, traveling at 10 mph is a good speed. A wounded soldier is most likely going to be suffering from some level of shock. The last thing he needs is to have his condition exacerbated by high-speed movement.

The Dynamic Balancing Behavior (DBB) in its legs enables the BEAR to adjust to a variety of positions and still maintain its mobility with the tracks on its legs (see Figure 1). Each leg can adjust independently. This is particularly useful for carrying a wounded soldier over rough terrain or up and down a flight of stairs. The BEAR's torso can rotate so that it can go through a doorway while carrying its precious life-ebbing cargo.

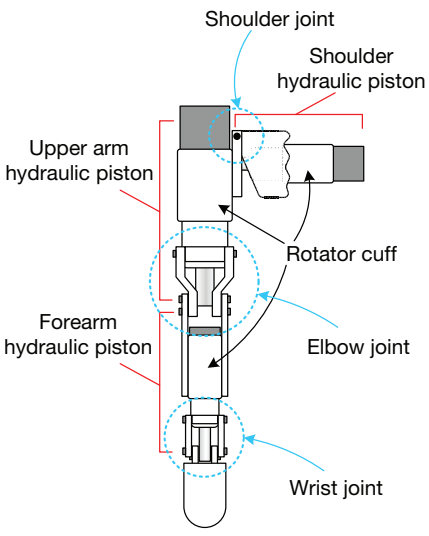


Note: Drawing is not to scale and may not represent actual implementation.

Figure 1

BEARing the weight

In order to provide enough power to lift heavy objects, the BEAR is designed with a hydraulic upper body. The hydraulics are similar to the hydraulics used in earth movers such as an excavator. Using hydraulic-powered arms, the BEAR is capable of lifting up to 600 lbs.[2] Each arm consists of three hydraulic pistons (see Figure 2). The first piston is located in the forearm. The forearm hydraulic piston controls the wrist flexion and wrist extension. The second piston is located in the upper arm and performs the basic functions of elbow flexion and elbow extension similar to the biceps brachii and triceps brachii muscles in the human body. The third piston is connected to the shoulder and located within the chest cavity. This piston simulates the lateral movement that the lateral deltoid provides humans. In addition, each piston can be rotated. With the rotational capabilities, each arm has six degrees of freedom in movement.



Note: Drawing is not to scale and may not represent actual implementation.

Figure 2

The BEAR responds to commands

Usually, when people think about robots, two extremes come to mind: the completely mindless machines that have been programmed to do one thing repetitively – and the machine with a mind of its own (for example, HAL 9000, "Transformers"). The BEAR hits the middle ground when it comes to autonomy. When given a command, the BEAR will proceed to carry it out. To issue commands, a Joint Architecture for Unmanned Systems (JAUS) compliant Operator Control Unit (OCU) is needed. The OCU being developed by Vecna is based on the VIA Nano-ITX EPIA-NL5000[3].

The BEAR's Heads-Up Display (HUD) will be seen on the OCU, so the human operator can see and hear what is in the BEAR's environment. Data about the BEAR's environment is captured through its cameras and microphones and transmitted to the OCU. The current version of the OCU employs a gamepad

Another role for BEAR

Because the characteristics of strength and endurance can be designed into robots, BEAR can also be suitable for lugging support gear such as extra ammunition, weapons, repair kits, communications equipment, and so on. Standard army gear consists of items such as an M16A2 rifle, M9 pistol, M9 bayonet, Alice frame pack, and extra cartridges of ammunition. Together all of these items (with a fully loaded pack) could weigh more than 70 lbs. Extra ammunition is heavy and can easily add weight. It would be ideal if every squad had at least two robots: one for carrying gear and the other for assisting the medic.

to control the BEAR's actions. For example, if a user wanted the BEAR to pick up a box, the user would either type or select the 'pick up' command from its repertoire of commands, and then click on the item in the HUD. Future versions of the OCU may include voice commands. The human operator can also communicate with a casualty through the BEAR's microphone and speaker system.

Hope for the future

The BEAR is still in the development stages. Currently, it is in its sixth prototype. But when the final product is ready (estimated to be field ready in 2015), it will take on one of the biggest problems of war – casualties. Aside from its usefulness in military situations, the BEAR will also be useful in civilian applications such as the healthcare industry or as part of search and rescue firefighting teams. ■

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3. "VIA EPIA NL-Series Nano-ITX Board," VIA Technologies Website. 2008. VIA Technologies, Inc. 24 Mar. 2008 www.via.com.tw/en/products/mainboards/motherboards.jsp?motherboard_id=361.

John Lin *is a senior technical writer at VIA Technologies, Inc., based in Taipei, Taiwan. He has seven years of experience in the computer industry, with five-plus years at VIA. John graduated with a bachelor's degree in Business Economics from UCSB. He can be reached at JohnLin@via.com.tw.*

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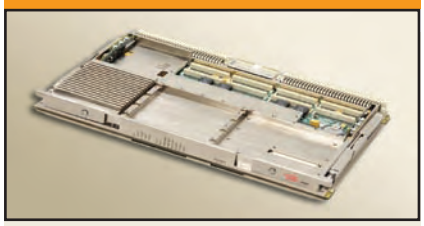
6U VME Intel Core 2 Duo SBC



The SVME-1901 SBC supports one Intel Core 2 Duo processor designed for benign and rugged air-cooled systems. The SVME-1901 acts as a dual CPU 6U VME64x air-cooled board; with the addition of a SCSI, SATA, or USB hard drive, the SVME-1901 becomes a full-featured computing platform. It supports the Windows XP, Solaris10, and Wind River GPP Linux 2.6 OSs. It has support for a clock calendar and NVRAM from a system-supplied battery backup and/or onboard capacitor. A user-programmable operating frequency allows dynamic, user-controlled power consumption adjustment. SVME-1901 supports extensive I/O on the faceplate including video graphics. Optional dual video displays are supported with rear I/O configurations. Onboard SCSI is provided for legacy systems that require SCSI storage solutions.

www.cwcembedded.com

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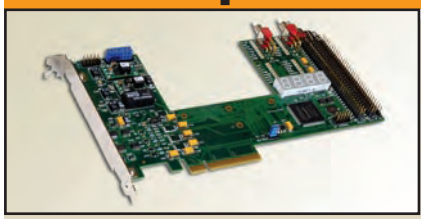
PCI Express-to-XMC adapter



The 5277 is an XMC-to-PCI Express adapter with metering function—a development/diagnostics tool that permits the testing of an XMC card in a PCI Express slot (1x, 4x, 8x, or 16x). It also can be used to measure XMC current and voltages and PCI Express bus frequency. Due to the vertical orientation of the mounted XMC, a user has ready access to both sides of the card. All signals on the XMC P16 connector are accessible via two 64-pin headers. PCI Express lanes on the P15 XMC connector are routed to the PCI Express edge finger connector. Adapter provides +12 V or +5 V for VPWR to the XMC card and is jumper selectable.

www.technobox.com

TECHNOBOX

6U VME CPU board

The VSBC-6848 is a 6U VME CPU board with a PowerQUICC II MPC8248 processor rated at 760 DMIPS at 400 MHz. Additional features include SDRAM on socket, 16 MB flash, hardware encryption unit, SODIMM 64-bit SDRAM up to 512 MB, 1 MB SRAM, and a CompactFlash socket for rugged onboard storage. If more storage is needed, an optional Dual Serial-ATA controller gives access to large-volume storage drives. For communication, the board includes two Fast Ethernet ports; two HDLC ports with ESD-protected, software-programmable RS-232, RS-422, and RS-485 interfaces; one USB port; and one RS-232 console port. The VSBC-6848 includes its own hardware encryption processor. Additional functionality is available through two 32-bit PMC extension slots and eight general-purpose TTL I/Os. One nonvolatile 256 Kb EEPROM is available for user parameters. The board is compatible with the VME specification Revision C and requires only 5 V power supply, with less than 1.5 A of current. It also supports a complete VME 32 interface for master and slave accesses with bus arbiter, interrupt handler, and DMA controller functions.

www.actis-computer.com

ACTIS COMPUTER

COTS Ethernet and USB I/O solutions provide bus independence

By Earle Foster and Wallace Krebs

Adding general purpose I/O to PMC and VME system buses can present some challenges. These include limited COTS I/O module diversity and a lack of open slots for I/O devices. External I/O devices however, are allowing designers to expand beyond the traditional bus-based design options. Among these devices are Ethernet and USB I/O solutions, which make adding I/O painless.

System designers face several challenges when adding general purpose I/O to system buses such as PMC and VME. The most obvious and common barrier is the limited diversity of COTS I/O modules for these bus types. This often translates into a cost issue when custom products are required. Another common barrier is the lack of open slots for the I/O devices.

Fortunately, designers can select the best SBC for their application and then adopt external I/O devices to expand beyond traditional bus-based design choices. The best solution is to use Ethernet and USB I/O devices. The vast majority of CPU modules provide Ethernet and USB interfaces, and I/O manufacturers offer a wide variety of these products to support various instrumentation and control requirements. By using Ethernet and USB I/O devices, engineers can design their core system architecture without concern for I/O expansion and can realize the cost effectiveness of these widely available I/O devices.

Distribute I/O anywhere using Ethernet

Interfacing I/O using Ethernet is becoming a popular trend for many reasons. Most SBCs provide at least one Ethernet port and are commonly connected to a network; therefore, interfacing them to Ethernet I/O devices is a natural choice. The networked I/O modules can be placed closer to the signals being monitored, which greatly simplifies field wiring. Another benefit of many Ethernet I/O products is the ability to access them from any authorized host computer on the network.

Ethernet serial servers make adding RS-232, RS-422, and RS-485 communication ports simple using virtually any Ethernet port. Adding more ports is as easy as connecting another serial server. Application software can use a COM port redirector software that allows serial ports to appear as virtual COM ports to the host machine. Using this approach, standard serial operating calls are transparently redirected to the serial server. In turn, this guarantees compatibility with legacy serial devices and enables backward compatibility with existing software. For more precise control, application software can communicate directly to the serial ports using raw socket mode. One example of these serial servers is Sealevel Systems' SeaLINK family, ranging from 1 to 16 ports.

Digital and analog I/O signals are also easily interfaced using off-the-shelf, Ethernet-connected devices. Some Ethernet I/O products take advantage of the Modbus TCP protocol to simplify software development and provide interoperability with other Modbus I/O devices. Modbus TCP transports Modbus data packets using the standard TCP/IP protocol, and many third party test and measurement software applications provide support. Acromag markets a family of Modbus TCP-compatible analog I/O devices such as the BusWorks 900EN Series with modules offering analog input and output interfaces to voltage and current signals. The modules are compact and mount on DIN rail for easy installation in an instrumentation cabinet.

> "Designing an effective I/O solution for a VME or PMC system can present unexpected obstacles. The traditional approach of adding separate I/O ... can leave engineers frustrated."

I/O connectivity via USB

Developed for use with desktop peripherals, USB is now commonly used for connecting I/O in industrial and OEM applications. USB is fast and, since the introduction of USB 2.0, can achieve a raw data rate of 480 Mbps. Many SBCs have external USB ports with standard USB Type A connectors and often include convenient internal header connectors with two or more USB ports. This makes USB devices easy to implement. However, the point-to-point nature of USB can limit the implementation options for I/O-intensive applications.

One solution for addressing this USB port limitation is to interface multiple modules from a single USB port with USB data acquisition products. Each I/O module can connect to the host with a locking, high-retention USB Type B connector that eliminates accidental disconnection. Modules can include an RS-485 Modbus RTU downstream port for connecting additional expansion modules. This allows up to 246 Modbus RTU I/O expansion modules to be daisy-chained together to achieve the required I/O count using a single USB host connection. Each module is assigned a unique Modbus address that can be set by hardware switch or via software. The host computer uses the standard Modbus protocol to communicate with these modules. Offerings such as Sealevel Systems' SeaI/O USB data acquisition products (Figure 1) can facilitate this process.

Figure 1

External I/O options expand traditional bus-based design choices

Designing an effective I/O solution for a VME or PMC system can present unexpected obstacles. The traditional approach of adding separate I/O bus boards for serial, digital, and analog I/O expansion can leave engineers frustrated with the lack of selection and high cost of these bus-based products. Another common concern when adding expansion boards is the availability of backplane slots.

System designers now have options that extend beyond the typical backplane add-in board. Using COTS Ethernet and USB I/O solutions allows valuable rack space to be reserved for ever-increasing disk capacity, communications, DSP, and other bandwidth-critical expansion requirements. Ethernet and USB I/O solutions are fast, simplify field wiring, and streamline repairs and upgrades. The broad availability of serial, digital, and analog I/O products from a variety of manufacturers usually proves more flexible and cost effective than PMC and VMEbus expansion boards, which makes USB and Ethernet I/O devices the optimal solution. ■

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Wallace Krebs *is lead of product marketing and SEO/SEM efforts at Sealevel Systems, Inc. Wallace has more than 15 years' technical experience in midrange and commercial computing with a background in mechanical engineering. He can be reached at Wallacek@sealevel.com.*

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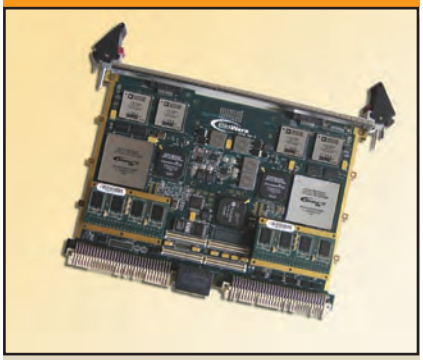
6U VXS card



The GT-6U-VME (GTV6) is a conduction-cooled 6U VXS card. The GTV6 features two Altera Stratix II GX FPGAs (2SGX90 or 130), two processing clusters consisting of two ADSP-TS201S TigerSHARC DSPs from Analog Devices, and up to 3 GB of DDR2 SDRAM memory. The GTV6 is used for high-end, multiprocessing applications and existing and future military applications requiring embedded signal processing in a VXS/VITA 41 form factor.

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BITTWARE

Remote-controlled switch sensor

The SwitchNet is a remote-controlled, relay operated AC power switch-sensor framework that offers power measurement and can be controlled over the Intranet/Internet. Suitable for remote power control, rebooting computers remotely, security, and control. SwitchNet features include intelligent power measurement and management, control interface over browser-based application, direct telnet, and programmable API. Additionally, critical alerts configure the system to take critical actions such as powering off all or specific devices based on local and remote feedback loops from sensors.

www.embeddedmachines.com

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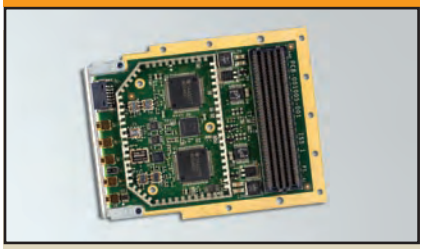
Dual-channel FMC



The ADC510 is a dual-channel 500 MSps 12-bit ADC FPGA Mezzanine Card (FMC) based on the VITA 57.1 standard. It enables developers to integrate FPGAs and analog input into their embedded system designs. Applications include SIGnals INTelligence (SIGINT), Electronic Counter Measures (ECM), and radar. The FMC utilizes two Texas Instruments ADS5463 ADC devices with each device supporting a sampling rate up to 500 MSps and providing 12 bits of digital output. The high-bandwidth connectivity of the FMC interface ensures that data can be transferred to the FPGA without compromising throughput. ADC510 is supported by VMETRO's XF suite, which includes software APIs for remote hosts, HDL examples, and air- and conduction-cooled rugged variants.

www.vmetro.com

VMETRO

Software radio PMC module

Pentek's Model 7151 is a high-performance, high-resolution software radio PMC module well suited for GSM cell-phone monitoring and SIGnals INTelligence (SIGINT) applications. It includes four 200 MHz 16-bit A/D converters that feed a proprietary FPGA IP core, delivering 256 channels of digital down conversion. The module features four RF/IF inputs digitized at 200 MSps with 16-bit resolution, along with 256 DDC channels independently tunable across four 100 MHz bands. In addition, Model 7151 provides highly optimized Virtex-5 FPGA technology and flexible assignment of A/Ds to DDC channels. Software and software support packages are available for Linux, Windows, and VxWorks.

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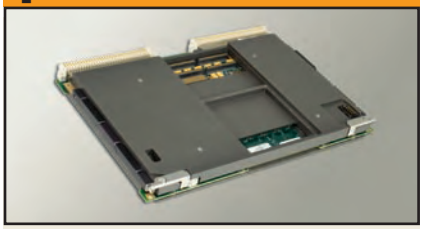
Server-level performance SBC



The VX6-200R/C VXS SBC features include dual Intel dual-core Xeon processors, Intel E7520 memory controller hub, and PMC-X/XMC site. Dual DDR-400 memory interfaces access up to 4 GB of memory, and four GbE ports are standard. The architecture supports four-way Symmetric Multiprocessing (SMP), which provides performance advantages for compute-intensive applications while requiring minimal software porting. Supports optional SVGA video with onboard ATI RAGE Mobility M graphics chip. Air-cooled and conduction-cooled versions are available.

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USM main XMC mezzanine card

The P699 is an XMC mezzanine card for any compliant host carrier board in any type of bus system, such as CompactPCI, PXI, VME, or on any type of stand-alone SBC. Features include main XMC for Universal Submodules (USMs), PCIe 2.5 Gbps, 1 FPGA 24,624 LE (for user-defined I/O and Nios soft core), 32 MB DDR2 SDRAM, and 4 MB flash. The P699 uses robust connectors to the USM. (The USM concept was developed for harsh environments.) Meanwhile, all other components are soldered. The card operates at temperature ranges of -10 °C to +70 °C screened.

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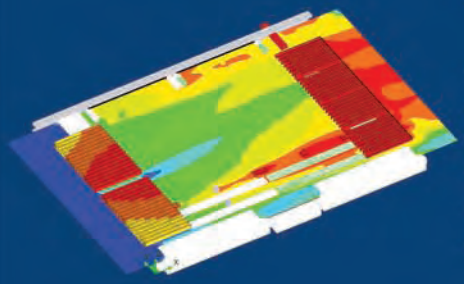

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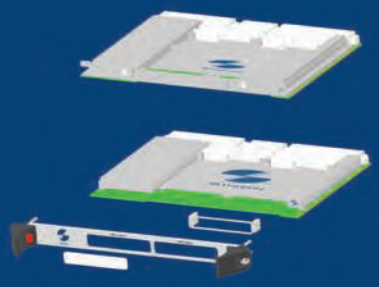

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Critical systems on small platforms need ultra-compact computing

By Thomas Roberts

Defense imaging systems are beginning to deploy advanced sensor technology on small, often unmanned, platforms. Constrained by platform size, systems designers must still transform an unrelenting sensor data stream into information that fits into the bandwidth available for data transmission. To meet this challenge, designers need a new generation of rugged, ultra-compact, and powerful real-time computers.

Sophisticated, sensor-based imaging systems have become critical military assets, providing invaluable intelligence on battlefields around the globe. However, the timely use of that intelligence is impacted by bandwidth limitations in the data links that provide the transmission backbone from a sensor platform to a ground station.

Improvements in data communications will not be sufficient to meet this challenge, as systems will be overwhelmed by the information data streams from new generations of sensors. Hyperspectral Imaging (HSI) and Laser Radar (LADAR) will augment, but not replace, the Electro-Optic Infrared (EO/IR) and Synthetic Aperture Radar (SAR) sensors used today. As data links increase in bandwidth, they will continue to lag behind the breadth and depth of new, sophisticated sensors.

Imaging systems can address the challenge by using computing technology to make better use of existing data-link bandwidth. Processing power co-located on the sensor platform can be used first to turn raw data into images, then for image compression, and, at the most sophisticated level, to execute image exploitation algorithms such as change detection in comparing two images. Each level requires more computing power but enables the data link to be used more efficiently to transmit useful information.

While sensor systems are always hungry for more compute power, another trend makes it difficult to deliver: Sensor platforms are becoming increasingly smaller. Over the past decade, defense forces have found Unmanned Vehicles (UVs) with sophisticated sensors to be extremely valuable intelligence-gathering assets, carrying out long missions without crew fatigue and, most importantly, greatly reducing risks to military personnel. Now that UVs have proven their value, the current trend is to build new generations of smaller vehicles, including airborne, ground-based, or undersea platforms.

To maximize small-platform effectiveness, they must carry the same sophisticated sensors currently deployed in large platforms, not just basic imaging systems such as the video cameras that currently constitute many airborne payloads. Technology organizations are, in fact, making smaller sensors – and now they need ultra-compact computing resources *next to the sensor* so data can be turned into images that can fit onto the available transmission bandwidth. Packaging technology is also key in these ultra-compact computers.

Requirements for small, deployable computers

The trend toward smaller, unmanned platforms is driven partly by cost, but more significantly by changes in threat. Next-generation platforms will operate in a more lethal battlefield environment brought about by the worldwide proliferation of advanced detection technology. Using multiple, smaller platforms offers a greater likelihood of system survivability than a single, large platform.

While needs vary across a range of implementations, requirements for these next-generation embedded computing systems can be summarized as follows:

On the order of 100 GFLOPS

Systems can be implemented with less than 100 GFLOPS of processing power, but image-exploitation algorithms such as change-detection, geo-registration, or automatic target recognition demand that level of processing or more.

Less than 10 pounds

Case in point: There is a tactical category of smaller unmanned aerial vehicles with a total payload capacity ranging from 60 to 200 lbs. In a general sense, it is reasonable to allocate up to 10 lbs. of that payload capacity to computing, but not much more.

Smaller than ATR-sized

The ATR system for standardized electronics packaging evolved to meet the needs of deployment in manned aircraft. New generations of UVs are not built to fit human dimensions, so it is not surprising that the ATR form factor, even in its half-ATR short form, is simply too big.

Flexible enough to support a range of I/O protocols

An embedded computing system that is processing sensor input must be flexible enough to support multiple types of sensors. Sensor payloads can change from one type to another, or use multiple types within one payload. For example, an EO/IR set of sensors used for a daylight operation may be replaced by a Thermal Night Imaging System (TNIS) for a mission in darkness, while a SAR sensor is used simultaneously for both missions. Supporting this type of sensor flexibility translates into a need for a mission computing system that can support multiple I/O protocols.

Surviving extreme environments

Defense electronics systems must perform in harsh environmental conditions including excessive heat, humidity, poor air quality, high altitude, shock, and vibration. These embedded computers must not overheat, even when temperatures range up to 55 °C and the air is too thin to be used for cooling. At the same time, they must possess the mechanical integrity to withstand high shock and vibration forces.

Figure 1

A sample shock specification for rugged applications is 50 *g* z-axis, 80 *g* x-y-axis, 11 ms half-sine, with a corresponding vibration specification of 0.04 *g*2/Hz, based on 20-2,000 Hz, 1 hr/axis.

Small form factors meet the challenge

While the requirements are formidable, advances in processing elements can be utilized to create solutions. Multicore processors and FPGAs can be used to accelerate computing, often in a complementary fashion. New computing enclosures, rugged, sealed, and using liquid-cooled sidewalls, allow these processing elements to be deployed in extremely small spaces.

For example, the recently announced PowerBlock50 from Mercury Computer Systems (Figure 1) is a fully integrated, ultra-compact embedded computer. To meet the first requirement of sensor computing – high performance – it features a modular architecture that allows for flexible configuration of multiple processors, delivering well over 100 GFLOPS of processing power via PowerQUICC III, Xilinx Virtex-4, or Intel processors. A PCI Express switch-fabric backplane is used for high-bandwidth interconnection between modules.

This processing power is packed into an ultra-compact and lightweight package. A fully configured PowerBlock50 weighs less than 7 lbs. and measures only 4.1" x 5.3" x 5.8" (105 mm x 134 mm x 148 mm). It can be held comfortably in one hand. State-of-the-art liquid cooling efficiently removes heat at any altitude, and rugged features include locking modules for shock and vibration immunity, EMI isolation, and more.

Future view: Small platforms, small computers

A new generation of small, defense-imaging platforms demands correspondingly small computing systems. The challenge is to meet this demand without compromising performance, flexibility, or survivability. Creative designs using new computing and small form factor packaging technology make it possible. ■

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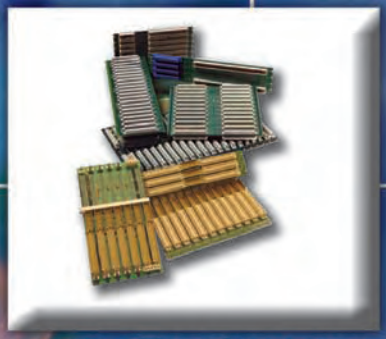

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The PMC-MC-X2-Chassis is designed to work with the PMC-MC-X2 dual PMC mini carrier. The carrier and chassis make it easy to use the PMC stack with power supply, slot zero functions, and fans. Its small size is slightly larger than a PMC, and PMCs are stacked. The mini carrier has a built-in power supply for the +12 V, -12 V, +5 V, and +3.3 V rails and is highly efficient and fuse protected. Built-in-slot zero functions include bus arbitration, interrupt routing, reset, and clock distribution with 33/66 selection. The fans are PrPMC controlled or always on. Twin 3.8 CFM fans are positioned to maximize air across the PMCs.

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VPX SERDES test modules

Elma Electronic's Serializer/Deserializer (SERDES) modules are designed to plug into VPX backplanes and directly test the channel compliance. They can be used to test VPX switch and node cards and/or the backplane channels without requiring external equipment or special test fixtures. Plugging directly into the backplane/chassis, modules allow characterization of signals and eliminate the need for SMA connectors, cables, and measurement hardware. The user can plug the cards into the test chassis, connect the USB cable to a laptop, download the GUI software, and begin measurements. The first in the test module series is an eight-channel version for 6U cards. SERDES test technology deployed in the VPX test modules can be affixed to various form factor carrier boards. A module kit includes software with a simple GUI interface.

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XMC graphics subsystem

Pinnacle Data System's XMC-E24D module is a high-performance dual display graphics subsystem designed for processor boards with an XMC mezzanine card interface. Using the ATI Radeon E2400 controller, the module enables compatible CompactPCI, AdvancedTCA, or VME blades in military, industrial, and other critical applications to take advantage of AMD's advanced graphics technology. The two displays (DVI, VGA, or dual-channel LVDS) can have independent refresh rates, resolutions, and color controls, offering great flexibility.

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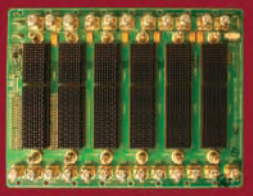
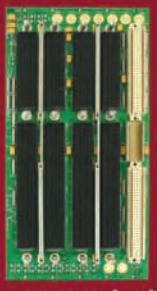
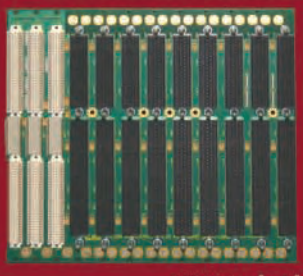


3U VPX

6U VPX



VPX Hybrid



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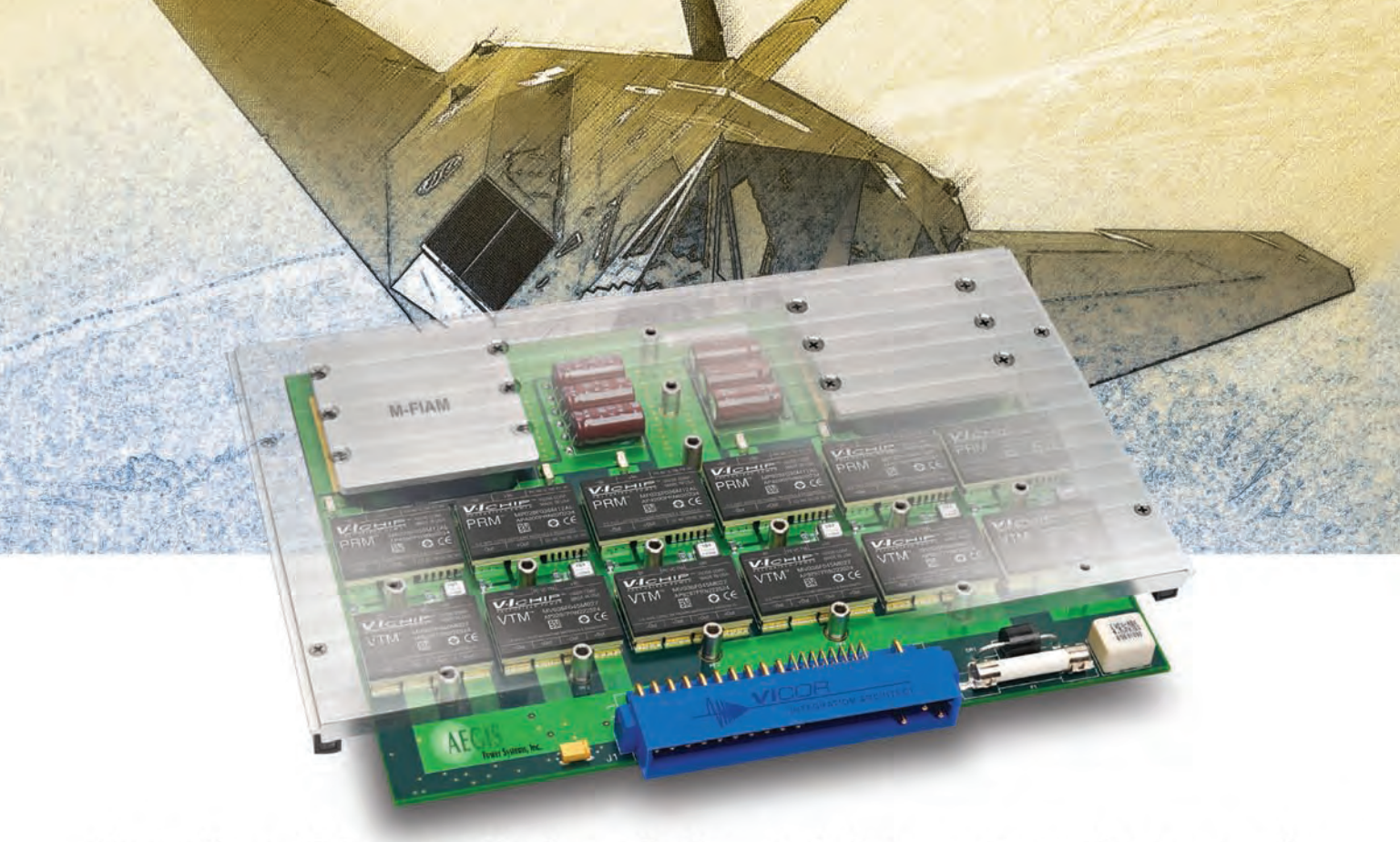

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- Single slot VME
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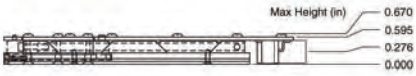

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